EE 271 – Introduction to Digital Circuits and Systems
HW #2 - Due 27 January

1.) For the following Verilog code, draw the corresponding circuit diagram for “bigMod”. Your circuit should only involve standard gates (AND, OR, NAND, NOR, XOR, Inverter), and the variable names Val, X, Y, and Z. DO NOT SIMPLIFY THE CIRCUIT. Note: all of the code is legal Verilog, with no errors.

```verilog
module tstMod(F, A, B, C);
    output F;
    input A, B, C;
    assign F = A | (~B & C);
endmodule

module bigMod(Val, X, Y, Z);
    output Val;
    input X, Y, Z;
    wire T;
    tstMod T1 (.F(T), .A(1), .B(X), .C(Y));
    tstMod T2 (.F(Val), .A(Z), .B(X), .C(T));
endmodule
```

2.) For the following circuits, put them into minimized Sum of Products forms by using a K-map.

a.) \( (A \oplus D) \cdot \overline{C} + B \cdot (A \cdot B + \overline{C} \cdot D) \) Remember, \( \oplus = XOR \). Also, to evaluate complex equations you can use a truth table, and evaluate subfunctions first.

b.) \( \overline{A} \cdot \overline{B} \cdot C \cdot D + \overline{C} \cdot D \cdot (A + \overline{B}) + A \cdot \overline{B} \cdot (C + \overline{D}) + \overline{A} \cdot B \cdot C \cdot D \)

3.) A 4-input minority gate is, a function that is TRUE when most of its inputs are FALSE, and FALSE when most of its inputs are TRUE. Ambiguous situations should be treated as “Don’t Cares”. Using a K-Map, produce the minimum Sum of Products form for this circuit. If there is more than one possible solution to the K-map, pick one.

4.) For each of the Boolean expressions given below, use K-maps to provide a minimized sum of products.

a.) \( F = \overline{B} \cdot (A \oplus C) + AB + \overline{ABC} \)

b.) \( F = B \cdot (C + D) + D \cdot (A + B) + \overline{CD} \cdot (A + B) + AB \cdot \overline{D} \)

5.) Using the expressions from the previous problem, provide a circuit diagram using only NAND gate. You may use inverters as necessary, but your circuit should be as efficient as possible.
6.) For the circuit given below, show the output ("F") waveform for the transition (A=0, B=1, C=0) to (A=1, B=1, C=0). All gates (inverters, ANDs, ORs, XORs) have a delay of 5ns.