EE 471 – Computer Design and Organization
Winter 2015

Instructor: Prof. Scott Hauck (hauck@ee.washington.edu) EE-307Q
Office hours: by appointment (email w/schedule).

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Office hours (Room 361/371) up-to-date times on website


Recommended: Frank Vahid & Roman Lysecky Verilog for Digital Design is also recommended.

Topics Covered: Introduction to computer architecture, algorithms, hardware design for various computer subsystems, CPU control unit design, memory organization, cache design, and virtual memory.

Prerequisites: CSE 143, EE 271. Strong knowledge of hardware design and Verilog from 271 is essential.

Assignments: The major goals of the class are to familiarize you with basic structure of microprocessors. As part of this, students will develop a Verilog implementation of a simple RISC microprocessor based upon the MIPS instruction set. Note that the labs GROW SIGNIFICANTLY in the amount of time it takes to complete them. The average time to complete the labs is expected to be:

<table>
<thead>
<tr>
<th>Lab</th>
<th>Description</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lab 1</td>
<td>Register File</td>
<td>12 hours</td>
</tr>
<tr>
<td>Lab 2</td>
<td>ALU</td>
<td>11 hours</td>
</tr>
<tr>
<td>Lab 3</td>
<td>Single-cycle CPU</td>
<td>25 hours</td>
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<tr>
<td>Lab 4</td>
<td>Pipelined CPU</td>
<td>34 hours</td>
</tr>
</tbody>
</table>

Exams: There will be one midterm (2/18) and one final exam (8:30-10:20 Mon 3/16).

Grade: The grade will be determined by the following approximate weights: homeworks (15%), design project (40%), midterm (20%), final exam (25%).

Outline: The class will have the following approximate schedule. Material may be added or dropped based on class timing and progress.

* Introduction to processor architecture.
* Assembly language programming.
* Computer Arithmetic.
* Performance measures.
* Processor Datapaths & Control.
* Pipelining.
* Memory hierarchy, caches, virtual memory.
* Advanced topics in computer architecture.

Website: http://www.ee.washington.edu/class/471/hauck/