EE 541 – Automated Layout of Integrated Circuits

Autumn 2015

Instructor: Prof. Scott Hauck  (hauck@uw.edu)  EE-307Q
Office hours by appointment (email with your availability).


Topics Covered: Basic algorithms for VLSI Physical Design, including partitioning, floorplanning, placement, and routing.

Prerequisites: Good knowledge of programming in at least one of C, C++, or Java, including data structures such as graphs and linked lists (CSE 373, CSE 326, or equivalent). The basics of Boolean logic and circuit diagrams (EE 271 or equivalent).

Assignments: The major goals of the class are to familiarize you with basic algorithms for the various steps in the physical design process. To aid in this process, students will be provided with a framework for a set of CAD tools written in Java. Over the course of the quarter each student will complete this framework to produce a complete, integrate CAD tool suite.

All programming assignments will be completed in Java. However, since the majority of the system is already written for you, students will not need to know the more complex aspects of the Java language. The portions of Java students will need to know is virtually identical to C/C++ in concept and syntax, and students will learn those aspects of Java they need over the first few weeks of the quarter.

No prior experience with Java is required.

Late work will be penalized 10% for 24 hours late, 30% for 48 hours late, 60% for 72 hours late, and not accepted beyond that.

Exams: There will be one final exam (12/15 4:30-6:20) and no midterm.

Grade: The grade will be determined by the following approximate weights: programming assignments (35%), written homework (25%), final exam (30%), and class participation (10%).

Outline: The class will have the following approximate schedule. Material may be added or dropped based on class timing and progress.

**Week 1:** Introduction to the Physical Design flow. Algorithm background, including Computational Complexity, NP-completeness, and Heuristic algorithms.

**Week 2:** Basic fabrication steps. Transistor implementations of CMOS logic gates. Logic implementation alternatives. The graph representation of circuits.

**Week 3:** Partitioning

**Week 4:** Floorplanning

**Week 5:** Placement

**Week 6:** Global Routing

**Week 7:** Detailed Routing

**Week 8:** Compaction

**Week 9:** FPGA Physical Design

Website: http://www.ee.washington.edu/class/541/hauck/