SUGGESTION: Sit down and do the following in about an hour. These are representative exam questions, and should take less than an hour to complete (a real exam would be longer).

1.) To limit the number of swap moves in force-directed placement, our (not-so) crack team of programmers have come up with the following pseudo-code:

```plaintext
make_best_nonswap_move ()
{
    int bestX, bestY;
    node bestNode = null;
    float bestDist = chip_width*chip_height;

    foreach node N {
        for (x = 1 to chip_width) {
            for (y = 1 to chip_height) {
                if (occupied[x][y] == 0) {
                    float dist = abs(x-optimalX[N]) + abs(y-optimalY[N]);
                    if (dist < bestDist) {
                        bestX = x;
                        bestY = y;
                        bestNode = N;
                        bestDist = dist;
                    }
                }
            }
        }
    }
    occupied[bestX][bestY] = bestNode;
}
```

Find the Big-O of this program. You can assume that the abs() function is O(1), and the chip_width and chip_height both equal approximately $\sqrt{V}$, where $V$ is the number of nodes in the circuit.
2.) Apply the complete left-edge algorithm (with dog-legs) to the following channel. Show all graphs you create as part of the process.
3.) Assume that all Inverters have a delay of 1ns, AND gates are 2ns, registers 0ns. Create the retiming graph for this structure and a desired clock period of 3ns. Then, draw the circuit after retiming is applied.
4.) For the following circuit, do ONE PASS (iteration) of the Fiduccia-Mattheyses algorithm. List each node moved (in order) and the cutsize achieved after that move. Also, draw the state of the circuit (the partitioning) at the beginning of the next iteration. Each partition is allowed to contain AT MOST 5 nodes.

Node Moved  Cutsize
Partitioning before next iteration: