Global Routing Abstraction - Routing Regions

Only need overall direction of routes (details done later)
Break routing area into rectangular regions

Global Routing Abstraction - Channels & Switchboxes

Regions are now broken into “channels” and “switchboxes”
   channels can have terminals on two (opposite) sides
   switchboxes can have terminals on all four
Detailed router does better on “channels” - maximize channels in decomposition
   Region order of routing can maximize # of channels instead of switchboxes
Graph Model

Can represent the routing structure as a graph
Label nodes with capacity, edges with distances

Extending Grid Routers to Graph Model

Route source to destination via breath-first/steiner.
Length at each step is distance from routing region centers
Remove vertical and/or horizontal capacity in channels along route
Do not route through regions without appropriate capacity
Fixed vs. Variable Capacities

Structured ASIC, FPGA: Capacity fixed by placement
- Decrement capacity as you route, when saturated must route elsewhere

Standard Cells: Can increase height of routing channel, width of feedthroughs
- Increment required capacity as you route, and route entire circuit
- Set all capacities as “free routing” demands
- Iterate while reducing critical sizes

Ordering Nets

In general, nets routed earlier are routed better than nets routed later
- Changing capacity forces nets away from good locations

Ordering heuristics
- Net fanout (large fanout nets harder to route well)
- Net criticality (nets on critical path more important to route well)

Note: hard to get a good order. May need to iterate, moving “difficult” nets earlier in the ordering.
Order Independent Routing

Can avoid order dependency by iterating:
Until good routing found {
    Route nets independent of congestion
    Add “penalty” to over-capacity regions
}

Diagram showing a grid with labeled nodes A to E and I to W, with some nodes marked as 1, 2, 3, or 4, and a line connecting nodes B and D.