

Scott Alan Hauck

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Personal

Born May 4, 1968. US citizenship. Married to Susan Elizabeth Hauck, daughter Lindsey Madison Hauck and son Quinn Cameron Hauck.

Education

Ph.D., Computer Science & Engineering, University of Washington, 1995.

Thesis: *Multi-FPGA Systems*

Advisors: Prof. Gaetano Borriello and Prof. Carl Ebeling.

M.S., Computer Science & Engineering, University of Washington, 1992.

B.S., Electrical Engineering & Computer Science, University of California – Berkeley, 1990.

Research Interests

Domain-Specific FPGAs, Reconfigurable Computing Architectures, Compilers, and Applications, FPGA Architectures and CAD tools, Logic Emulation, VLSI Design and CAD, Compression, Hardware for Floating Point Computations, Nanotechnology.

Awards

Finalist, U.W. Distinguished Teaching Award, 2008.

Best Paper Award, Microelectronic Systems Education Conference, 2007.

Elixent, Inc. S.O.A.P.-Star: Spot On Award Program (employee achievement award), 2006.

Alfred P. Sloan Research Fellow (2001)

U.W. EE Department's Outstanding Research Advisor Award 2001.

Senior Member, IEEE (2001)

NSF CAREER award (1999)

1999 IEEE Circuits and Systems Society Transactions on VLSI Systems Best Paper Award

Northwestern University, ECE Department's Best Teacher of 1998/99

June and Donald Brewer Junior Professorship, (Northwestern chair, given up in move to U.W.) 1999-2001

AT&T Bell Laboratories Graduate Fellowship

Berkeley Honors Society

National Merit Finalist

Nominated, U.W. College of Engineering Faculty Innovator for Teaching, 2007, 2008.

Nominated, U.W. Distinguished Teaching Award, 2004, 2007, 2008.

Nominated, U.W. College of Engineering Outstanding Faculty Member, 2004.

Nominated, U.W. EE Department's Faculty Service Award, 2004.

Nominated, U.W. EE Department's Outstanding Research Advisor Award 2003, 2004, 2008.

Nominated, U.W. EE Department's Teaching Award 2001, 2003, 2007.

Awards (to advisees)

College of Engineering Community Innovators Teaching Assistant Innovator Award to Ken Eguro (2008)

College of Engineering Dean's Undergraduate Research Award to Jimmy Xu (2008)

Yang Research Award to Akshay Sharma (2005)

National Science Foundation Fellowship Honorable Mention to Michael Beauchamp (2003 & 2004)

Mary Gates Endowment for Students research training grant to Henry Lee (2003).

Intel Fellowship to Mark Chang (2002)

Lincoln Labs Fellowship to Shawn Phillips (2002)

Cabell Thesis Year Fellowship to Katherine Compton (2002)

U.W. EE Department's Outstanding Research Assistant Award to Mark Chang (2001-2002)
National Science Foundation Fellowships to Katherine Compton (1998), Mark Holland (2001)
1999 Motorola UPR Best Paper Award (to student Katherine Compton)

Employment

University of Washington, Seattle, WA

9/08 – current Professor.
9/00 – 9/08 Associate Professor.
9/99 – 9/00 Assistant Professor.

Elixent, Ltd, Bristol, England.

8/05 – 6/06 Senior Research Engineer.

Northwestern University, Evanston, IL

10/95 – 9/99 Assistant Professor.

University of Washington, Seattle, WA

3/91 - 9/95 Research Assistant. Investigated multi-FPGA systems, rapid-prototyping, asynchronous design. Developed FPGA architectures. Helped write Orca-C portable parallel programming language.
10/90 - 3/91 Teaching Assistant for Intro. to A.I. & Intro. to Operating Systems

University of California – Berkeley, Berkeley, CA

1/90 - 5/90 Reader. Graded for CS170 – Intro. to Computer Science Theory
1/87 - 5/89 Senior Engineering Aid. Participated in the design and development of the PICASSO user interface for the POSTGRES database project.

I.B.M. – T. J. Watson Research Center, Hawthorne, NY

6/89 - 12/89 Temporary Employee – Co-op. Built a framework and toolkit for a set of X11-based Common Lisp programming tools. System was distributed commercially by Lucid, Inc. as *XLT*.

Bell Communications Research (Bellcore), Morristown, NJ

6/88 - 8/88 Technical Summer Intern. Helped with a Broadband ISDN feasibility study.

Publications

Journal Articles

S. Hauck, S. Burns, G. Borriello, C. Ebeling, "An FPGA For Implementing Asynchronous Circuits", *IEEE Design & Test of Computers*, Vol. 11, No. 3, pp. 60-69, Fall 1994.

S. Hauck, "Asynchronous Design Methodologies: An Overview", *Proceedings of the IEEE*, Vol. 83, No. 1, pp. 69-93, January 1995.

G. Borriello, C. Ebeling, S. Hauck, S. Burns, "The Triptych FPGA Architecture", *IEEE Transactions on VLSI Systems*, Vol. 3, No. 4, pp. 491-501, December 1995.

C. Ebeling, L. McMurchie, S. Hauck, S. Burns, "Placement and Routing Tools for the Triptych FPGA", *IEEE Transactions on VLSI Systems*, Vol. 3, No. 4, pp. 473-482, December 1995.

S. Hauck, G. Borriello, "An Evaluation of Bipartitioning Techniques", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 16, No. 8, pp. 849-866, August 1997.

S. Hauck, G. Borriello, "Pin Assignment for Multi-FPGA Systems", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 16, No. 9, pp. 956-964, September 1997.

S. Hauck, "The Roles of FPGAs in Reprogrammable Systems", *Proceedings of the IEEE*, Vol. 86, No. 4, pp. 615-639, April 1998.

S. Hauck, G. Borriello, C. Ebeling, "Mesh Routing Topologies for Multi-FPGA Systems", *IEEE Transactions on VLSI Systems*, Vol. 6, No. 3, pp. 400-408, September, 1998.

S. Hauck, Z. Li, E. J. Schwabe, "Configuration Compression for the Xilinx XC6200 FPGA", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 8, pp. 1107-1113, August, 1999.

- M. Enos, S. Hauck, M. Sarrafzadeh, "Evaluation and Optimization of Replication Algorithms for Logic Bipartitioning", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 18, No. 9, pp. 1237-1248, September, 1999.
- S. Hauck, M. M. Hosler, T. W. Fry, "High Performance Carry Chains for FPGAs", *IEEE Transactions on VLSI Systems*, Vol. 8, No. 2, pp. 138-147, April 2000.
- S. Hauck, "FPGA Tools Need Hardware Assistance", *EE Times*, February 16th, 2001.
- K. Compton, S. Hauck, "Reconfigurable Computing: A Survey of Systems and Software", *ACM Computing Surveys*, Vol. 34, No. 2, pp. 171-210. June 2002.
- K. Compton, Z. Li, J. Cooley, S. Knol, S. Hauck, "Configuration Relocation and Defragmentation for Run-time Reconfigurable Computing", *IEEE Transactions on VLSI Systems*, Vol. 10, No. 3, pp. 209-220, June 2002.
- K. Compton, S. Hauck, "Research Focuses on Application-Specific Reconfigurable Blocks", *EE Times*, September 11th, 2002.
- S. Hauck, T. W. Fry, M. M. Hosler, J. P. Kao, "The Chimaera Reconfigurable Functional Unit", *IEEE Transactions on VLSI Systems*, Vol. 12, No. 2, pp. 206-217, February 2004.
- M. L. Chang, S. Hauck, "Précis: A User-Centric Word-Length Optimization Tool", *IEEE Design & Test of Computers*, Vol. 22, No. 4, pp. 349-361, July-August 2005.
- T. Fry, S. Hauck, "SPIHT Image Compression on FPGAs", *IEEE Transactions on Circuits and Systems for Video Technology*, Vol. 15, No. 9, pp. 1138-1147, September 2005.
- K. Eguro, S. Hauck, "Resource Allocation for Coarse Grain FPGA Development", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 24, No. 10, pp. 1572-1581, October 2005.
- A. Sharma, C. Ebeling, S. Hauck, "PipeRoute: A Pipelining-Aware Router for Reconfigurable Architectures", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 25, No. 3, pp. 518-532, March 2006.
- M. Holland, S. Hauck, "Automatic Creation of Domain-Specific Reconfigurable CPLDs for SoC", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 26, No. 2, pp. 291-295, February 2007.
- K. Compton, S. Hauck, "Automatic Design of Area-Efficient Configurable ASIC Cores", *IEEE Transactions on Computers*, Vol. 56, No. 5, pp. 662-672, May 2007.
- M. J. Beauchamp, S. Hauck, K. D. Underwood, K. S. Hemmert, "Architectural Modifications to Enhance the Floating-Point Performance of FPGAs", *IEEE Transactions on VLSI Systems*, Vol. 16, No. 2, pp. 177-187, February 2008.
- K. Compton, S. Hauck, "Automatic Design of Reconfigurable Domain-Specific Flexible Cores", *IEEE Transactions on VLSI Systems*, Vol 16, No. 5, pp. 493-503, May 2008.
- S. Phillips, A. Sharma, S. Hauck, "Layout Generation for Domain-Specific FPGAs", submitted to *IEEE Transactions on VLSI Systems*.
- K. Eguro, S. Hauck, "Enhancing Routing Heuristics on Pipelined-FPGAs", submitted to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.
- M. Haselman, S. Hauck, "The Future of Integrated Circuits: A Survey of Nano-electronics", submitted to *Proceedings of the IEEE*.
- K. Compton, S. Hauck, "Track Placement: Orchestrating Routing Structures to Maximize Routability", in preparation for *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*.

Patents, Theses, Books and Book Chapters

S. Hauck, G. Borriello, S. Burns, C. Ebeling, "Field-Programmable Gate Array for Synchronous and Asynchronous Operation", U.S. Patent 5,367,209, issued November 22, 1994.

J. A. Brzozowski, S. Hauck, C.-J. H. Seger, "Chapter 15: Design of Asynchronous Circuits", in J. A. Brzozowski, C.-J. H. Seger, *Asynchronous Networks*, Springer-Verlag, 1995.

S. Hauck, Multi-FPGA Systems, Ph.D. Thesis, University of Washington, Dept. of CS&E, September, 1995.

A. C. Miguel, R. E. Ladner, E. A. Riskin, S. Hauck, D. K. Barney, A. R. Askew, A. Chang, "Predictive Coding of Hyperspectral Images", in G. Motta, F. Rizzo, J. A. Storer (editors), *Hyperspectral Data Compression*, Springer Science & Business Media, Inc: NY, pp. 197-232, 2006.

S. Hauck, "Field-Programmable Gate Arrays", *McGraw-Hill Encyclopedia of Science & Technology*, 10th edition, 2006.

S. Hauck, "Field-Programmable Gate Arrays", *McGraw-Hill Yearbook of Science & Technology*, 2007, pp. 81-84.

M. Haselman, S. Hauck, T. Lewellen, R. Miyaoka, "Data Acquisition System for a Positron Emission Tomography Scanner", *U.S. Provisional Patent Application No. 60/985,083*, November 2, 2007.

K. Eguro, S. Hauck, "Enhancing Timing-Driven FPGA Placement for Pipelined Netlists", *U.S. Provisional Patent Application No. 61/012,728*, December 10, 2007.

S. Hauck, A. DeHon (editors), *Reconfigurable Computing: The Theory and Practice of FPGA-based Computation*, Morgan Kaufmann/Elsevier, 2008.

Student Theses

M. Enos, *Replication for Logic Partitioning*, Master's Thesis, Northwestern University, Dept. of EECS, 1996.

O. Stone, *A Comparison of ASIC Implementation Alternatives*, Master's Thesis, Northwestern University, Dept. of ECE, 1996.

M. Hosler, *High Performance Carry Chains for FPGAs*, Master's Thesis, Northwestern University, Dept. of ECE, 1997.

G. Gu, *Accelerating Photoshop Applications with Reconfigurable Hardware*, Master's Thesis, Northwestern University, Dept. of ECE, 1999.

M. Chang, *Adaptive Computing in NASA Multi-Spectral Image Processing*, Master's Thesis, Northwestern University, Dept. of ECE, 1999.

K. Compton, *Programming Architectures for Run-Time Reconfigurable Systems*, Master's Thesis, Northwestern University, Dept. of ECE, 1999.

T. Fry, *Hyperspectral Image Compression on Reconfigurable Platforms*, Master's Thesis, University of Washington, Dept. of EE, 2001.

M. Richmond, *A Lemple-Ziv based Configuration Management Architecture for Reconfigurable Computing*, Master's Thesis, University of Washington, Dept. of EE, 2001.

C. Mulpuri, *Runtime and Quality Tradeoffs in FPGA Placement and Routing*, Master's Thesis, Northwestern University, Dept. of ECE, 2001.

S. Phillips, *Automatic Layout of Domain Specific Reconfigurable Subsystems for System-on-a-Chip*, Master's Thesis, Northwestern University, Dept. of ECE, 2001.

A. Sharma, *Development of a Place and Route Tool for the RaPiD Architecture*, Master's Thesis, University of Washington, Dept. of EE, 2001.

M. Holland, *Harnessing FPGAs for Computer Architecture Education*, Master's Thesis, University of Washington, Dept. of EE, 2002.

Z. Li, *Configuration Management Techniques for Reconfigurable Computing*, Ph.D. Thesis, Northwestern University, Dept. of ECE, 2002.

K. Eguro, *RaPiD-AES: Developing an Encryption-Specific FPGA Architecture*, Master's Thesis, University of Washington, Dept. of EE, 2002.

T. Owen, *Unequal Loss Protection of Hyperspectral Compressed Images on Reconfigurable Platforms*, Master's Thesis, University of Washington, Dept. of EE, 2003.

K. Compton, *Architecture Generation of Customized Reconfigurable Hardware*, Ph.D. Thesis, Northwestern University, Dept. of ECE, 2003.

M. Chang, *Variable Precision Analysis for FPGA Synthesis*, Ph.D. Thesis, University of Washington, Dept. of EE, 2004.

S. Phillips, *Automating Layout of Reconfigurable Subsystems for Systems-on-a-Chip*, Ph.D. Thesis, University of Washington, Dept. of EE, 2004.

M. Haselman, *A Comparison of Floating Point and Logarithmic Number Systems on FPGAs*, Master's Thesis, University of Washington, Dept. of EE, 2005.

A. Sharma, *Place and Route Techniques for FPGA Architecture Advancement*, Ph.D. Thesis, University of Washington, Dept. of EE, 2005.

M. Holland, *Automatic Creation of Product-Term-Based Reconfigurable Architectures for System-on-a-Chip*, Ph.D. Thesis, University of Washington, Dept. of EE, 2005.

M. Beauchamp, *Architectural Modifications to Enhance the Floating-Point Performance of FPGAs*, M.S. Thesis, University of Washington, Dept. of EE, 2006.

P. Grossman, *Benchmarking the Independence Architecture Adaptive Placer on the Triptych FPGA Architecture*, M.S. Thesis, University of Washington, Dept. of EE, 2006.

D. DeWitt, *An FPGA Implementation of Statistical Based Positioning for Positron Emission Tomography*, M.S. Thesis, University of Washington, Dept. of EE, 2008.

B. Weintraub, *Building BLAST for Coprocessor Accelerators Using Macah*, Honors Project, University of Washington, Dept. of CSE, Spring 2008.

Conference and Symposium Papers

S. Hauck, G. Borriello, C. Ebeling, "TRIPTYCH: An FPGA Architecture with Integrated Logic and Routing", *Advanced Research in VLSI and Parallel Systems: Proceedings of the 1992 Brown/MIT Conference*, pp. 26-43, March, 1992.

S. Hauck, G. Borriello, C. Ebeling, "Mesh Routing Topologies for Multi-FPGA Systems", *International Conference on Computer Design*, pp. 170-177, October, 1994.

S. Hauck, G. Borriello, "Logic Partition Orderings for Multi-FPGA Systems", *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, pp. 32-38, February, 1995.

S. Hauck, G. Borriello, "An Evaluation of Bipartitioning Techniques", *Chapel Hill Conference on Advanced Research in VLSI*, pp. 383-402, March, 1995.

S. Hauck, T. W. Fry, M. M. Hosler, J. P. Kao, "The Chimaera Reconfigurable Functional Unit", *IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 87-96, 1997.

M. Enos, S. Hauck, M. Sarrafzadeh, "Replication for Logic Bipartitioning", *International Conference on Computer-Aided Design*, pp. 342-349, 1997.

- S. Hauck, "Configuration Prefetch for Single Context Reconfigurable Coprocessors", *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, pp. 65-74, 1998.
- S. Hauck, M. M. Hosler, T. W. Fry, "High Performance Carry Chains for FPGAs", *ACM/SIGDA International Symposium on Field-Programmable Gate Arrays*, pp. 223-233, 1998.
- S. Hauck, Z. Li, E. J. Schwabe, "Configuration Compression for the Xilinx XC6200 FPGA", *IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 138-146, 1998.
- S. Hauck, S. Knol, "Data Security for Web-based CAD", *Design Automation Conference*, pp. 788-793, 1998.
- S. Hauck, "The Future of Reconfigurable Systems", Keynote Address, *5th Canadian Conference on Field Programmable Devices*, Montreal, June 1998.
- Z. Li, S. Hauck, "Don't Care Discovery for FPGA Configuration Compression", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, pp. 91-98, 1999.
- M. L. Chang, S. Hauck, "Adaptive Computing in NASA Multi-Spectral Image Processing", *Military and Aerospace Applications of Programmable Devices and Technologies International Conference*, 1999.
- Z. A. Ye, N. Shenoy, S. Hauck, P. Banerjee, A. Moshovos, "CHIMAERA: A Tightly-Coupled Reconfigurable Unit/High-Performance Processor Architecture", *International Symposium on Computer Architecture*, pp. 225-235, 2000.
- Z. Li, K. Compton, S. Hauck, "Configuration Cache Management Techniques for FPGAs", *IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 22-36, 2000.
- P. Banerjee, N. Shenoy, A. Choudhary, S. Hauck, C. Bachmann, M. Haldar, P. Joisha, A. Jones, A. Kanhare, A. Nayak, S. Periyacheri, M. Walkden, D. Zaretsky, "A MATLAB Compiler for Distributed, Heterogeneous, Reconfigurable Computing Systems", *IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 39-48, 2000.
- C. Mulpuri, S. Hauck, "Runtime and Quality Tradeoffs in FPGA Placement and Routing", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, pp. 29-36, 2001.
- Z. Li, S. Hauck, "Configuration Compression for Virtex FPGAs", *IEEE Symposium on FPGAs for Custom Computing Machines*, 2001.
- K. Compton, S. Hauck, "Totem: Custom Reconfigurable Array Generation", *IEEE Symposium on FPGAs for Custom Computing Machines*, 2001.
- A. Lenharth, R. Ladner, S. Hauck, E. Riskin, A. Miguel, "Wavelet Compression of MODIS Satellite Images", *Earth Science Technology Conference*, August, 2001.
- T. Wu, A. C. Miguel, E. A. Riskin, A. E. Mohr, R. E. Ladner, S. Hauck, "Protecting regions of interest in medical images in a lossy packet network," in *Medical Imaging 2002: PACS and Integrated Medical Information Systems: Design and Evaluation*, Eliot L. Siegel, H. K. Huang, Editors, *Proceedings of SPIE*, Vol. 4685, 137-148 (2002).
- Z. Li, S. Hauck, "Configuration Prefetching Techniques for Partial Reconfigurable Coprocessor with Relocation and Defragmentation", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, pp. 187-195, 2002.
- S. Phillips, S. Hauck, "Automatic Layout of Domain-Specific Reconfigurable Subsystems for System-on-a-Chip", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, pp. 165-173, 2002.
- T. Fry, S. Hauck "Hyperspectral Image Compression on Reconfigurable Platforms", *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 251-260, 2002.
- M. L. Chang, S. Hauck, "Précis: A Design-Time Precision Analysis Tool", *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 229- 238, 2002.
- S. Hauck, M. L. Chang "Précis - A Design-Time Precision Analysis Tool", *Earth Science Technology Conference*, June, 2002.

- S. Hauck, T. W. Fry, "Hyperspectral Image Compression on Reconfigurable Platforms", *Earth Science Technology Conference*, June, 2002.
- K. Compton, A. Sharma, S. Phillips, S. Hauck, "Flexible Routing Architecture Generation for Domain-Specific Reconfigurable Subsystems", *International Conference on Field Programmable Logic and Applications*, pp. 59-68, 2002.
- A. Sharma, C. Ebeling, S. Hauck, "PipeRoute: A Pipelining-Aware Router for FPGAs", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, pp. 68-77, 2003.
- K. Eguro, S. Hauck, "Issues and Approaches to Coarse-Grain Reconfigurable Architecture Development", *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 111-120, 2003.
- A. C. Miguel, A. Chang, R. E. Ladner, S. Hauck, E. A. Riskin, "On-Board Satellite Implementation of Wavelet-Based Predictive Coding of Hyperspectral Images", *Earth Science Technology Conference*, 2003.
- M. Chang, S. Hauck, "Variable Precision Analysis for FPGA Synthesis", *Earth Science Technology Conference*, 2003.
- K. Compton, S. Hauck, "Track Placement: Orchestrating Routing Structures to Maximize Routability", *International Conference on Field Programmable Logic and Applications*, 2003.
- K. Compton, S. Hauck, "Flexibility Measurement of Domain-Specific Reconfigurable Hardware", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, pp. 155-161, 2004.
- A. Sharma, K. Compton, C. Ebeling, S. Hauck, "Exploration of Pipelined FPGA Interconnect Structures", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, pp. 13-22, 2004.
- A. C. Miguel, A. R. Askew, A. Chang, S. Hauck, R. E. Ladner, E. A. Riskin, "Reduced Complexity Wavelet-Based Predictive Coding of Hyperspectral Images for FPGA Implementation", pp. 469-479, *Data Compression Conference*, 2004.
- M. Chang, S. Hauck, "Automated Least-Significant Bit Datapath Optimization for FPGAs", *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 59-67, 2004.
- M. Holland, S. Hauck, "Automatic Creation of Reconfigurable PALs/PLAs for SoC", *International Conference on Field Programmable Logic and Applications*, pp. 536-545, 2004.
- S. Phillips, A. Sharma, S. Hauck, "Automating the Layout of Reconfigurable Subsystems Via Template Reduction", *International Conference on Field Programmable Logic and Applications*, pp. 857-861, 2004.
- S. Phillips, S. Hauck, "Automating the Layout of Reconfigurable Subsystems Using Circuit Generators", *IEEE Symposium on Field-Programmable Custom Computing Machines*, 2005.
- M. Haselman, M. Beauchamp, A. Wood, S. Hauck, K. Underwood, K. Scott Hemmert, "A Comparison of Floating Point and Logarithmic Number Systems for FPGAs", *IEEE Symposium on Field-Programmable Custom Computing Machines*, 2005.
- K. Eguro, S. Hauck, A. Sharma, "Architecture-Adaptive Range Limit Windowing for Simulated Annealing FPGA Placement", *Design Automation Conference*, pp. 439-444, 2005.
- M. Holland, S. Hauck, "Automatic Creation of Domain-Specific Reconfigurable CPLDs for SoC", *International Conference on Field Programmable Logic and Applications*, pp. 95-100, 2005.
- A. Sharma, C. Ebeling, S. Hauck, "Architecture-Adaptive Routability-Driven Placement for FPGAs", *International Conference on Field Programmable Logic and Applications*, pp. 427-432, 2005.
- A. Sharma, S. Hauck, "Accelerating FPGA Routing Using Architecture-Adaptive A* Techniques", *IEEE International Conference on Field Programmable Technology*, pp. 225-232, 2005.
- K. Eguro, S. Hauck, "Armada: Timing-Driven Pipeline-Aware Routing for FPGAs", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, pp. 169-178, 2006.

M. J. Beauchamp, S. Hauck, K. D. Underwood, K. S. Hemmert, "Embedded Floating Point Units in FPGAs", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, pp. 12-20, 2006.

M. Holland, S. Hauck, "Improving Performance and Robustness of Domain-Specific CPLDs", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, pp. 50-59, 2006.

M. J. Beauchamp, S. Hauck, K. Underwood, K. S. Hemmert, "Architectural Modifications to Improve Floating-Point Unit Efficiency in FPGAs", *International Conference on Field Programmable Logic and Applications*, pp. 515-520, 2006.

Allan Carroll, Stephen Friedman, Brian Van Essen, Aaron Wood, Benjamin Ylvisaker, Carl Ebeling, Scott Hauck, "Designing a Coarse-grained Reconfigurable Architecture for Power Efficiency", *Department of Energy NA-22 University Information Technical Interchange Review Meeting*, 2007.

Ken Eguro, Scott Hauck, "Enhancing Timing-Driven FPGA Placement for Pipelined Netlists", to appear in *Design Automation Conference*, 2008.

Ken Eguro, Scott Hauck, "Simultaneous Retiming and Placement for Pipelined Netlists", to appear in *IEEE Symposium on Field-Programmable Custom Computing Machines*, 2008.

Workshop Papers

C. Ebeling, G. Borriello, S. Hauck, D. Song, E. A. Walkup, "Triptych: A New FPGA Architecture", *Oxford Workshop on Field-Programmable Logic and Applications*, September, 1991. Also appearing in W. Moore, W. Luk, Eds., *FPGAs*, Abingdon, England: Abingdon EE&CS Books, pp. 75-90, 1991.

E. A. Walkup, S. Hauck, G. Borriello, C. Ebeling, "Routing-directed Placement for the Triptych FPGA", *ACM/SIGDA Workshop on Field-Programmable Gate Arrays*, February, 1992.

S. Hauck, G. Borriello, S. Burns, C. Ebeling, "Montage: An FPGA for Synchronous and Asynchronous Circuits", *2nd International Workshop on Field-Programmable Logic and Applications*, August, 1992. Also appearing in H. Grunbacher, R. W. Hartenstein, Eds., *Field-Programmable Gate Arrays: Architectures and Tools for Rapid Prototyping*, Berlin: Springer-Verlag, pp. 44-51, 1993.

S. Hauck, G. Borriello, C. Ebeling, "Mesh Routing Topologies for FPGA Arrays", *ACM/SIGDA 2nd International Workshop on Field-Programmable Gate Arrays*, February, 1994.

S. Hauck, G. Borriello, "Pin Assignment for Multi-FPGA Systems (Extended Abstract)", *IEEE Workshop on FPGAs for Custom Computing Machines*, pp. 11-13, April, 1994.

Conference & Workshop Posters

S. Hauck, G. Borriello, C. Ebeling, "Springbok: A Rapid-Prototyping System for Board-Level Designs", *ACM/SIGDA 2nd International Workshop on Field-Programmable Gate Arrays*, February, 1994.

S. Hauck, W. D. Wilson, "Abstract: Runlength Compression Techniques for FPGA Configurations", *IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 286-287, 1999.

K. Compton, J. Cooley, S. Knol, S. Hauck, "Abstract: Configuration Relocation and Defragmentation for FPGAs", *IEEE Symposium on FPGAs for Custom Computing Machines*, pp. 279-280, 2000.

M. Holland, J. Harris, S. Hauck, "Harnessing FPGAs for Computer Architecture Education", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, pg. 250, 2002.

S. Hauck, "APHYDS: Academic Physical Design Skeleton", *IEEE International Conference on Microelectronic Systems Education*, 2003.

M. Holland, J. Harris, S. Hauck, "Harnessing FPGAs for Computer Architecture Education", *IEEE International Conference on Microelectronic Systems Education*, 2003.

- M, Chang, S. Hauck, "Least-Significant-Bit Optimization Techniques for FPGAs", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, 2004.
- S. Phillips, A. Sharma, S. Hauck, "Automating the Layout of Reconfigurable Subsystems Via Template Reduction", *IEEE Symposium on Field-Programmable Custom Computing Machines*, pp. 340-341, 2004.
- A. Sharma, C. Ebeling, S. Hauck, "Architecture Adaptive Routability-Driven Placement for FPGAs", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, 2005.
- M. Holland, S. Hauck, "Automatic Creation of Domain-Specific Reconfigurable CPLDs for SoC", *IEEE Symposium on Field-Programmable Custom Computing Machines*, 2005.
- S. Hauck, "Active Learning Techniques in a CAD Course", *IEEE International Conference on Microelectronic Systems Education*, pp. 125-126, 2007.
- M. D. Haselman, S. Hauck, T.K. Lewellen, R.S. Miyaoka, "Simulation of Algorithms for Pulse Timing in FPGAs", *IEEE Nuclear Science Symposium and Medical Imaging Conference*, 2007.
- M. Haselman, R. Miyaoka, T. K. Lewellen, S. Hauck, "FPGA-Based Data Acquisition System for a Positron Emission Tomography (PET) Scanner", *ACM/SIGDA Symposium on Field-Programmable Gate Arrays*, 2008.
- T.K. Lewellen, R.S. Miyaoka, L.R. MacDonald, M. Haselman, S. Hauck, "Design of a Second Generation Firewire Based Data Acquisition System for Small Animal PET Scanners", submitted to *IEEE Nuclear Science Symposium and Medical Imaging Conference*, 2008.
- Don DeWitt, Robert S. Miyaoka, Xiaoli Li, Cate Lockhart, Tom Lewellen, Scott Hauck, "Design of an FPGA based Algorithm for Real-Time Solutions of Statistics-Based Positioning", submitted to *IEEE Nuclear Science Symposium and Medical Imaging Conference*, 2008.
- M.D. Haselman, S. Hauck, T.K. Lewellen, R.S. Miyaoka, "Digital Pulse Timing in FPGAs for Positron Emission Tomography", submitted to *IEEE Nuclear Science Symposium and Medical Imaging Conference*, 2008.

Workshop Reports

J. Cong et. al, *Final Report: NSF/NSC International Workshop on Challenges and Opportunities In Giga-Scale Integration For System-On-A-Chip*, Taiwan, August 1999.

Technical Reports

- S. Hauck, G. Borriello, C. Ebeling, "Achieving High-Latency, Low-Bandwidth Communication: Logic Emulation Interfaces", *University of Washington, Dept. of CSE Technical Report #95-04-04*, January 1995.
- S. Hauck, G. Borriello, C. Ebeling, "Springbok: A Rapid-Prototyping System for Board-Level Designs", 1995.
- S. Hauck, A. Agarwal, "Software Technologies for Reconfigurable Systems", *Northwestern University, Dept. of ECE Technical Report*, 1996.
- K. Compton, S. Hauck, "Mapping Methods for the Chimaera Reconfigurable Functional Unit", *Northwestern University, Dept. of ECE Technical Report*, 1997.
- S. Hauck, S. Knol, "Data Security for Web-based CAD", *Northwestern University, Dept. of ECE Technical Report*, 1998.
- S. Hauck, W. D. Wilson, "Runlength Compression Techniques for FPGA Configurations", *Northwestern University, Dept. of ECE Technical Report*, 1998.
- Z. A. Ye, N. Shenoy, S. Hauck, P. Banerjee, A. Moshovos, "A C Compiler for a Processor with a Reconfigurable Functional Unit", *Northwestern University, Dept. of ECE Technical Report*, 1999.
- Z. A. Ye, A. Moshovos, S. Hauck, N. Shenoy, P. Banerjee, "CHIMAERA: Integrating a Reconfigurable Functional Unit into a High-Performance, Dynamically-Scheduled Superscalar Processor", *Technical Report*, 1999.

P. Banerjee, A. Choudhary, S. Hauck, N. Shenoy, C. Bachmann, M. Chang, M. Haldar, P. Joisha, A. Jones, A. Kanhare, A. Nayak, S. Periyacheri, M. Walkden, "MATCH: A MATLAB Compiler for Adaptive Computing Systems", 1999.

K. Eguro, S. Hauck, "synFPGA: Application Specific FPGA Synthesis", *Northwestern University, Dept. of ECE Technical Report*, 2000.

K. Compton, J. Cooley, S. Knol, S. Hauck, "Configuration Relocation and Defragmentation for FPGAs", *Northwestern University, Dept. of ECE Technical Report*, 2000.

S. Hauck, Z. Li, "Improved Configuration Prefetch for Single Context Reconfigurable Coprocessors", *Technical Report*, 2000.

T. Owen, S. Hauck, "Arithmetic Compression on SPIHT Encoded Images", *University of Washington, Dept. of EE Technical Report UWEETR-2002-0007*, 2002.

M. Holland, J. Harris, S. Hauck, "Harnessing FPGAs for Computer Architecture Education", *University of Washington, Dept. of EE Technical Report*, 2002.

K. Eguro, S. Hauck, "Decipher: Architecture Development of Reconfigurable Encryption Hardware", *University of Washington, Dept. of EE Technical Report UWEETR-2002-0012*, 2002.

K. Compton, S. Hauck, "Track Placement: Orchestrating Routing Structures to Maximize Routability", *University of Washington, Dept. of EE Technical Report UWEETR-2002-0013*, 2002.

A. Sharma, C. Ebeling, S. Hauck, "PipeRoute: A Pipelining-Aware Router for FPGAs", *University of Washington, Dept. of EE Technical Report UWEETR-2002-0018*, 2002.

Z. Li, S. Hauck, "Don't Care Discovery for FPGA Configuration Compression", 2002.

Z. Li, S. Hauck, "Configuration Prefetching Techniques for Partial Reconfigurable Coprocessor with Relocation and Defragmentation", *Technical Report*, 2003.

Z. Li, K. Compton, S. Hauck, "Configuration Caching Management Techniques for Reconfigurable Computing", *Technical Report*, 2003.

Z. Li, S. Hauck, "Configuration Compression for Virtex FPGAs", *Technical Report*, 2004.

K. Eguro, S. Hauck, "Issues of Wirelength Cost Models in Routing-Constrained FPGAs", *University of Washington, Dept. of EE Technical Report UWEETR-2004-0006*, 2004.

A. C. Miguel, A. R. Askew, A. Chang, S. Hauck, R. E. Ladner, E. Riskin, "Reduced Complexity Wavelet-Based Predictive Coding of Hyperspectral Images for FPGA Implementation", *Technical Report*, 2004.

A. Sharma, K. Compton, C. Ebeling, S. Hauck, "Exploration of RaPiD-style Pipelined FPGA Interconnects", *Technical Report*, 2004.

M. Haselman, M. Beauchamp, A. Wood, S. Hauck, K. Underwood, K. Scott Hemmert, "A Comparison of Floating Point and Logarithmic Number Systems for FPGAs", *Technical Report*, 2005.

A. Sharma, C. Ebeling, S. Hauck, "Architecture-Adaptive Routability-Driven Placement for FPGAs", *Technical Report*, 2006.

S. Hauck, K. Compton, K. Eguro, M. Holland, S. Phillips, A. Sharma, "Totem: Domain-Specific Reconfigurable Logic", *Technical Report*, 2006.

M. Holland, S. Hauck, "Domain-Specific Reconfigurable PAL/PLA Creation for SoC", *Technical Report*, 2007.

B. Ylvisaker, A. Carroll, S. Friedman, B. Van Essen, C. Ebeling, D. Grossman, S. Hauck, "Macah: A "C-Level" Language for Programming Kernels on Coprocessor Accelerators", *Technical Report*, 2008.

Grants & Contracts

Funded

National Science Foundation, 6/97-5/99. Scott Hauck, Majid Sarrafzadeh, *Mapping Time Oriented Tools for Logic Emulation*, \$219,000 (including matching of \$75,000 from AT&T, \$25,000 from Northwestern).

Defense Advanced Research Projects Agency, 9/97-8/00. Scott Hauck, Prithviraj Banerjee, Majid Sarrafzadeh, *Architectures, Compilers, and Configuration Management for Mass-Market Adaptive Computing*, \$1,981,469.

National Science Foundation, CISE Research Infrastructure Program, 1997-2002. Prithviraj Banerjee, Alok Choudhary, Scott Hauck, D. T. Lee, Majid Sarrafzadeh, Peter Scheuermann, Valerie Taylor, *A Distributed High-Performance Computing Infrastructure*, \$906,512.

Motorola, University Partnership in Research Program, 9/97-8/02. Scott Hauck, *Dynamically Reconfigurable Hardware for Digital Signal Processing*, \$81,577.

National Science Foundation, Research Experiences for Undergraduates, 9/97-8/99. Scott Hauck, \$20,000.

Defense Advanced Research Projects Agency, 4/98-3/01. Prithviraj Banerjee, Alok Choudhary, Scott Hauck, Nagaraj Shenoy, *A MATLAB Compilation Environment For Adaptive Computing Systems*, \$1,855,662.

National Science Foundation, CAREER Program, 9/99-8/04. Scott Hauck, *Logic Emulation Infrastructure for Research and Teaching*, \$240,000.

National Aeronautics and Space Administration, 9/00-8/03. Scott Hauck, Prithviraj Banerjee, *MATLAB-Based Adaptive Computing for NASA Image Processing Applications*, \$758,358 (\$379,938 U.W. + \$309,835 Northwestern + \$68,585 NASA GSFC).

National Aeronautics and Space Administration, 9/00-8/03. Scott Hauck, Eve Riskin, *Reconfigurable Computing Based Compression for Spaceborne Hyperspectral Images*, \$642,043 (\$573,458 U.W. + \$68,585 NASA GSFC).

National Science Foundation, 9/00-8/05. David Allstot, Jeff Bilmes, Chris Diorio, Carl Ebeling, Scott Hauck, Hui Liu, Sumit Roy, Carl Sechen, Richard Shi, Mani Soma, *Heterogeneous System Integration in System-on-a-Chip Designs*, \$4,113,001 (incl. \$113,001 Supplement).

Xilinx, 9/00-6/01. Scott Hauck, *Compression Techniques for FPGA Configurations*, \$40,000.

Sloan Research Fellowship, 9/01-8/05. Scott Hauck, \$40,000.

National Science Foundation, CISE-RI Program, 9/01-8/07. Scott Hauck, David Allstot, Carl Ebeling, Carl Sechen, Mani Soma, Scott Dunham, Richard Shi, Greg Zick, *An Infrastructure for Integrated Systems Education and Innovation*, \$1,458,565 (\$872,490 NSF + \$295,075 Sun + \$291,000 UW Cost Sharing).

Sandia National Labs, 1/04-12/05. Scott Hauck, *Reconfigurable Hardware for Floating-Point Computations*, \$130,957.

Altera Inc, 11/04 – 8/05. Scott Hauck, *Architecture Adaptive Routability-Driven Placement for FPGAs*, \$26,623.

National Science Foundation, 11/04-10/08. Scott Hauck, *Achieving High-Performance Reconfigurable Computing in Commodity Devices*, \$325,000. Grant #CCF0426147.

U.W. – Royalty Research Fund, 1/05 – 1/06. Scott Hauck, *Self-Assembled Nano-FPGAs*, \$26,212.

National Institutes of Health, 2006-2011. Thomas K. Lewellen, Robert S. Miyaoka, Paul E. Kinahan, Marie Janes, Scott A. Hauck, *High Resolution Detectors for Oncology Applications*, \$1,895,000 (\$1,250,000 direct + \$645,000 indirect). Grant #R01 EB002117.

Department of Energy, 9/06 – 8/09. Carl Ebeling, Scott Hauck, *A High-Performance, Low-Power Configurable Fabric for Embedded Applications*, \$730,000. Grant #DE-FG52-06NA27507.

Zecotek Medical Systems, 3/06 – 2/11. Thomas K. Lewellen, Robert S. Miyaoka, Paul E. Kinahan, Scott A. Hauck, Marie Janes, *High Resolution Positron Emission Tomograph Detector and Electronics Development*, \$2,368,222.

Altera Inc, 1/07 – 12/07. Scott Hauck, Thomas K. Lewellen, *FPGA-Based Electronics for Advanced PET and PET/MRI Scanners*, \$20,000.

National Science Foundation, 10/07 – 9/10. Carl Ebeling, Scott Hauck, *Tools for Exploring Low-power, High-performance Reconfigurable Computing Architectures*, \$379,105.

Washington Technology Center, 7/08 – 6/09. Scott Hauck, Adam Alession, *Application and Benchmarking of Impulse C Technology to Medical Imaging Tasks*, \$120,000.

Department of Energy, 11/08 – 10/10. Robert Miyaoka, Thomas K. Lewellen, Scott Hauck, William Hunter, *A High Resolution Monolithic Crystal, DOI, MR Compatible, PET Detector*, \$606,314.

Pending

National Science Foundation, 10/08 – 9/11. Scott Hauck, *Multicore Optimized Routers for FPGAs*, \$372,673.

Donations

Funded

Xilinx, Donation of FPGA mapping software, 1996, \$28,050; 1997, \$5,925; 1998, \$5,725; 2000, \$41,948; 2002, \$3,990; 2005, \$700.

NSF/MOSIS, Donation of integrated circuit fabrication services for educational use, 1998, \$5,610.

Tektronix, Dollar match on oscilloscope, 2000, \$4,439.

Sun, Dollar match on ultra 5's, 2000, \$2,500.

Altera, Donation of FPGA mapping software, chips, and boards, 2006, \$28,220; 2007, \$7,980.

Professional Activities

Conference & Journal Organization

Associate Editor, International Journal of Reconfigurable Computing (IJRC), 2007 – present.

Guest Editor (with Toomas Plaks and others), ACM Transactions on Embedded Computing Systems, special issue on Configurable Computing: Configuring Algorithms, Processes, and Architecture, 2008.

Co-organizer, Cascadia Workshop on FPGAs, 2007.

Guest Editor (with Miriam Leeser and Russ Tessier), EURASIP Journal of Embedded Systems, special issue on Field-Programmable Gate Arrays in Embedded Systems, 2006.

Organizer, UBC/UW Workshop on FPGAs, 2005.

Associate Editor, IEEE Transactions on VLSI Systems, 1999 - 2001.

Program Chair, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2000.

General Chair, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2001.

Finance Chair, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2002.

Publicity Chair, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 1997-1999.

Steering Committee, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2000-present.

Topic Chair, Reconfigurable Architectures, International Workshop on Field Programmable Logic and Applications, 2008.

Sub-TPC Chair, Design Automation Conference, 2004.

Program Committee Member, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 1997-2003; IEEE Symposium on FPGAs for Custom Computing Machines (FCCM), 1997-2008; Design Automation Conference, 2003 - 2004; International Workshop on Field Programmable Logic and Applications, 2000, 2002-2005, 2007 - 2008; International Conference on Engineering of Reconfigurable Systems and Algorithms, 2004; Reconfigurable computing and FPGA conference (Reconfig), 2004, 2005, 2008; Workshop on Software Support for Reconfigurable Systems (ERSA), 2003; IEEE Microelectronic Systems Education Conference, 2003, 2005, 2007; IEEE International Conference on Field-Programmable Technology (FPT), Hong Kong, 2002-2004; Advanced Research in VLSI 2001, CORE-2000 - Reconfigurable Computing Workshop 2000; Great Lakes Symposium on VLSI, 1997.

Keynotes, Panels, Tutorials

Full Day Tutorial Organizer and Presenter, "Reconfigurable Systems: Logic Emulation, Custom Computing, and Beyond", Design Automation Conference, 1997.

Keynote Speaker, "The Future of Reconfigurable Systems", 5th Canadian Conference on Field Programmable Devices, Montreal, June 1998.

Panel Organizer and Moderator, "FPGAs in the Era of System-on-a-Chip", International Symposium on Field Programmable Gate Arrays, 1999.

Panel Member, "Architectures, Technologies and Design Methodologies for 2005 and Beyond", Military and Aerospace Applications of Programmable Logic Devices International Conference, 1999.

Panel Member, "Is Marriage in the Cards for Programmable Logic, Microprocessors and ASICs?", ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 2001.

Session Chair, Participant

Session Chair, ACM/SIGDA International Symposium on Field Programmable Gate Arrays, 1997, 1998, 2002, 2005; IEEE Symposium on FPGAs for Custom Computing Machines, 1997-2000, 2002 - 2005, 2007; International Symposium on Field-Programmable Logic, 2004.

Session Organizer, DAC 2003 - 2004.

Group Discussion Leader & Presenter, "Reconfigurable Device Architectures", Configurable Computing Workshop, Hewlett-Packard Labs, Bristol, England, 1998.

Participant, National Science Foundation Workshop on Research Directions for Next-Generation Systems Design and Integration, Seattle, WA, June 1999; NSF/NSC Joint Workshop on Challenges and Opportunities In Giga-Scale Integration for System-On-A-Chip, Taiwan, August 1999.

Reviewing

Reviewer, Proceedings of the IEEE, IEEE Transactions on Computers, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on VLSI Systems, IEEE Design & Test of Computers, Distributed Computing, NSF, ACM Transactions on Design Automation of Electronic Systems, Microelectronic Systems Education Conference, Design Automation Conference, Journal of VLSI Signal Processing Systems, International Symposium on Computer Architecture, IEEE Journal of Solid-State Circuits, U.W. RRF Program, National Sciences and Engineering Research Council of Canada, International Symposium on Microarchitecture, Journal of Signal Processing Systems, South Carolina DEPSCoR.

External Ph.D. Examiner, Mohammed Khalid, University of Toronto, 1998; Joerg Ritter, Martin-Luther-Universität, 2002; Benjamin Levine, CMU, 2004; Julien Lamoureux, University of British Columbia, 2007.

Miscellaneous

Member, ACM; Senior Member, IEEE.

Judge, Seattle Public Schools Middle School Science Fair, 2001, 2005.

IEEE Admission and Advancement Panel, November 15th, 2003.

Consulting

Motorola, Inc. Technology evaluation, October 1997.

Quickturn, Inc. Expert Witness, August 2000 – February 2003. *Mentor Graphics Corporation vs. Quickturn Design Systems, Inc. and Cadence Design Systems, Inc.*, U.S. District Court for the Northern District of California, Case No. C-00-03291 SI. March 2003 – September 2003. *Quickturn Design Systems, Inc. vs. Mentor Graphics Corporation and M2000*, 3rd Chamber, 2nd Section, of the Civil Court of Paris, France, Roll No. 98/21148.

Data Transit Corp. Expert Witness, May 2003 – June 2003. *I-Tech Corp. vs. Data Transit Corp, The Epoch Group, Inc., and Innotec Design, Inc.*, United States District Court, District of Minnesota, Civil Action No. 02-CV2765 (RHK/AJB).

Berkeley Law and Technology Group, LLC. Technology evaluation, July 2006 – October 2006.

Invention Law Group, PLLC. Technology evaluation, November 2006 – Ongoing.

Invited Presentations

Note: Does not include talks associated with conference presentations. External presentations by students are indicated by the name of the student who gave the presentation.

“An FPGA for Asynchronous Circuits”, U. of British Columbia, October 25, 1993.

“Multi-FPGA Systems”, Northwestern University, February 1995; Cornell University, March 1995; AT&T Bell Labs, March 1995; IBM – T. J. Watson Research Center, March 1995; University of California - Davis, March 1995; Yale University, April 1995; University of Illinois Urbana-Champaign, April 1995, Xilinx, Inc., April 1995; ARPA VLSI Contractors Meeting, April 1995; HP Inc., Boulder, May 1995; HP Labs, Bristol, England, August 21, 1995; UC Berkeley, February 14, 1996.

“An Introduction to Architectures, Compilers, and Configuration Management for Mass-Market Adaptive Computing”, DARPA ACS PI Meeting, November 1997.

“Triptych, Montage, Chimaera: Advanced FPGA Technologies”, Quicklogic Inc., November 10, 1997.

“Configuration Memory Management for Adaptive Computing Systems”, U. Illinois Chicago, January 23, 1998; U. Washington, January 30, 1998; UC Berkeley, April 17, 1998; Carnegie Mellon U., October 12, 1998; University of Toronto, December 11, 1998.

“Lessons Learned”, DARPA ACS PI Meeting, April 1998.

“FPGAs @ Northwestern”, Motorola, April 30, 1998; ECE Advisory Board, May 10, 1998.

Keynote Address, “The Future of Reconfigurable Systems”, 5th Canadian Conference on Field Programmable Devices, Montreal, June 1998.

“The Future of Reconfigurable Systems”, Carnegie Mellon U., October 14, 1998.

“Reconfiguration Architectures for Adaptive Computing Systems”, University of Washington, January 29, 1999.

“The Roles of Reconfigurable Logic in Systems-on-a-Chip”, Motorola, April 27, 1999.

“Teaching Engineering Concepts”, ECE Excellence in Teaching Seminar, Northwestern University, May 28, 1999.

“Reconfigurable Architectures, Applications, and CAD”, Graduate Research Seminar, Dept. of EE, University of Washington, October 15, 1999; Electrical Engineering Research Day, University of Washington, October 22, 1999. IEEE Brown Bag Lunch, University of Washington, October 27, 1999, Graduate Student Recruiting Day, University of Washington, March 6 & March 31, 2000.

“Panel: Research on the Internet and at the EE/CSE Interface”, Electrical Engineering Research Day, University of Washington, October 22, 1999.

“Architectures, Compilers, and Configuration Management for Mass-Market Adaptive Computing”, DARPA Program Review, April 3, 2000.

“Overview of the Chimaera Project”, DARPA PI Meeting, May 22, 2000.

“Research in Reconfigurable Systems”, U.W. Dept of EE Workshop for Korean Technology Visitors, July 18, 2000.

“The Chimaera Project”, ST Microelectronics, August 29, 2000.

“FPGA Configuration Management in the Chimaera Project”, DARPA PI Meeting, October 10, 2000.

“Totem: Domain-Specific Reconfigurable Subsystems for System-on-a-Chip”, Motorola Corporate Research, July 31, 2001. Quicksilver Inc., November 30, 2001.

“Variable Precision Analysis Tools”, NASA Goddard Teleconference, October 31st, 2001.

“Reconfigurable Computing Based Compression for Hyperspectral Images”, NASA Goddard Teleconference, October 31st, 2001.

“Precis: Variable Precision Analysis for FPGA-based Implementations”, NASA Goddard Teleconference, April 17th, 2002.

“Extending Reconfigurable Computing Based Compression to Unequal Loss Protection”, NASA Goddard Teleconference, April 17th, 2002.

“An Infrastructure for Integrated Systems Education and Innovation”, NSF CISE/EIA RIA and MII PI’s Workshop, July 13th, 2002.

“Enhanced FPGA-Based Hyperspectral Compression” NASA Goddard Site Review, August 21st, 2002.

“Totem: Domain-specific FPGA Generation”, Washington University, Dept. of CSE, October 11th, 2002.

“Compression on FPGAs”, Rapid Seminar, 2003.

“Totem: Domain-Specific FPGA Synthesis”, NSF ITR Site Visit, July 24th, 2003.

“Welcome”, EE Undergraduate Orientation, September 25th, 2003.

“The Time Management Freak Show”, ADVANCE Lunch, November 21st, 2003.

“Electrical Engineering” NSBE Department Panel, May 18th, 2004.

“Graduate School: Why & How”, U.W. – EE Undergraduates Grad School Panel, May 27th, 2004.

“Variable Precision Analysis for FPGA Synthesis”, Sandia National Labs, July 13th, 2004.

“Totem, The Rest of the Story...”, University of British Columbia, September 17th, 2004.

Akshay Sharma, Scott Hauck, “Architecture Adaptive A* Techniques for FPGA Routing”, *UW/UBC Workshop on FPGAs*, 2005.

Mike Haselman, Scott Hauck, “A Comparison of Floating Point and Logarithmic Number Systems on a FPGA”, *UW/UBC Workshop on FPGAs*, 2005.

Ken Eguro, Scott Hauck, "Architecture-Adaptive Range Limit Windowing for Simulated Annealing FPGA Placement", *UW/UBC Workshop on FPGAs*, 2005.

Mark Holland, Scott Hauck, "Automatic Creation of Domain-Specific CPLDs for System-on-a-Chip", *UW/UBC Workshop on FPGAs*, 2005.

"Hyperspectral Image Processing on FPGAs", UW CSE Configurable Computing Seminar, 2006.

Ken Eguro, Scott Hauck, "Pipelining Commodity Reconfigurable Devices", *UW/UBC Workshop on FPGAs*, 2006.

Mike Haselman, Scott Hauck, "An FPGA-Based PET Scanner", *UW/UBC Workshop on FPGAs*, 2006.

"The Time Management Freak Show", ADVANCE Lunch, March 2nd, 2007.

"Research in the ACME Lab", CSE Grad Student Visit Day, 2007.

"Reconfigurable Logic @ U.W.", Microsoft Research, 2007.

Mike Haselman, Scott Hauck, Tom Lewellen, Robert Miyaoka, "FPGA-Based Data Acquisition System for a PET Scanner", *Cascadia Workshop on FPGAs*, 2007.

Ben Ylvisaker, Scott Hauck, "Macah: Simplifying the Programming of Kernel Accelerators with Judicious Automation", *Cascadia Workshop on FPGAs*, 2007.

Brian Van Essen, Scott Hauck, "Molecular Dynamics Simulation for Hybrid Micro-Parallel Systems", *Cascadia Workshop on FPGAs*, 2007.

Ken Eguro, Scott Hauck, "Pipeline and Retiming-Aware Placement", *Cascadia Workshop on FPGAs*, 2007.

Allan Carroll, Stephen Friedman, Robin Panda, Brian Van Essen, Aaron Wood, Benjamin Ylvisaker, Carl Ebeling, Scott Hauck, "Designing a Coarse-grained Reconfigurable Architecture for Performance & Power Efficiency", U.W. Dept. of CSE Affiliates, 2007.

"Mosaic: High-Performance, Low-Power Configurable Fabrics for Embedded Applications", Department of Energy Site Visit, December 11th 2007.

"FPGAs for Tomography?", U.W. Dept. of Radiology Seminar, March 27th 2008.

Committees & Departmental Service

University of Washington (1999-current)

Computer Engineering Faculty Recruiting Committee, 2007 - 2008.

VLSI and Embedded Systems Curriculum Chair, 2007 – 2008.

EE Merit Review Committee, 2008.

EE Merit Review Committee, Chair of Assistant/Lecturer Subcommittee, 2008.

EE Curriculum Committee, 2003 – 2005, 2007 - 2008.

College Council on Educational Policy, 2007.

EE Server and Space Task Force, 2007.

Intel Fellowship review committee, 2007, 2008.

College Council, 2006.

UW Faculty Senate, 2004 – 2005.

EE Undergraduate Coordinator, 2003 - 2005.

EE Chair Search, 2003 – 2004, 2004 - 2005.

EE Faculty Advisory Board, 2000 - 2005.

College of Engineering Accreditation and Continuous Improvement (ACI) Committee, 2003 - 2005.

EE Admissions Committee, Committee Chair, 2003 - 2005.

University of Washington, Commencement Marshall, 2004, 2007, 2008.

EE Outstanding Staff Awards Committee, 2004.

EE Admissions Committee, 2003.

EE Undergraduate Scholarship Committee, Committee Chair, 2004 – 2005.

Chair, EE Ad Hoc Committee on Capstone courses, Committee Chair, 2003-2004.

EE Undergraduate Curriculum Construction Committee, 2002-2003.

EE Undergraduate Graduation Announcer, 2003 – 2004, 2007.

EE Computing Advisory Committee Chair, 2000-2002.

EE Computing Advisory Committee, 1999-2002.

EE Undergraduate Scholarship Committee, 2002.

Undergrad seminar, *Intro to “Digital”*, Oct 23rd, 2002; May 21st, 2003.

Civil Engineering Department Chair Search, 2001.

EE Strategic Planning Committee, 1999-2000.

Faculty Review Committee for Progress Toward Promotion, Jacob Rosen (2002), Katrin Kirchoff (2003 - 2004), Mark Holl (Chair, 2005), Larry McMurchie (Chair, 2005), Eric Klavins (2005), Brian Otis (2007), Brian Otis (Chair, 2008).

Graduate School Representative, Supervisory Committee: Scott Martin (ME, 2001 - 2003), Stephen P. Voght (Genetics, 2002 - 2007).

Supervisory Committee, Jovanka Ciric (EE 2001), Yoochang Chung (EE 2001-2002), Su Kio (EE 2001-2003), Jian Zhou (EE 2002-2003), Yi Han (EE 2002-2005), Sheng Sun (EE 2003-2006), Nuttorn Jangkrajarn (EE 2003-2006), Song Li (CSE 2004).

Quals Committee Member, Brian Van Essen (CSE 2006 - 2007)

Generals Committee Member, Ben Ylvisaker (CSE 2007).

Digital Systems Qualifying Exam Chair, Fall 2004, Fall 2007, Spring 2008.

Digital Systems Qualifying Exam Committee, Spring 2000, Fall 2000, Spring 2001, Fall 2002, Spring 2003, Fall 2004, Fall 2006.

Northwestern University (1995-1999)

EECS/ECE Computing Resources Committee, 1995-1998.

ECE Curriculum Committee, 1996-1998.

Graduate Electrical and Computer Engineering Students Society (GECES) Faculty Co-Advisor, 1997-1999.

Safety Committee Alternate Zone Warden, 1997-1998.

ECE Graduate Committee, 1998-1999.

Undergraduate Computer Engineering Program Committee, 1998-1999.

Computer Engineering Program of Study (POS) Committee Chairman, 1998-1999.

Teaching

University of Washington (Numbers are average of questions 1, 3 & 4. All scores are raw, not adjusted, as presented on the web.)

EE 271: Introduction to Digital Circuits and Systems (formerly 371)

Winter 2003. Q1 4.5, Q3 4.6, Q4 4.7, Ttl 4.6 (88th percentile in department)

Fall 2004. Q1 4.7, Q3 4.8, Q4 4.8, Ttl 4.8 (96th percentile in department)

Fall 2006. Q1 4.60, Q3 4.78, Q4 4.82, Ttl 4.7 (88th percentile in department)

Fall 2007. Q1 4.5, Q3 4.7, Q4 4.6, Ttl 4.6 (88th percentile in department)

EE 371: Introduction to Digital Circuits and Systems

Spring 2000. Q1 4.65, Q3 4.85, Q4 4.81, Ttl 4.77 (98th percentile in department, course prior ave 3.53)

Winter 2002. Q1 4.55, Q3 4.70, Q4 4.76, Ttl 4.67 (93rd percentile in department)

EE 471: Computer Design and Organization

Spring 2001. Q1 4.81, Q3 4.93, Q4 4.93, Ttl 4.89 (99th percentile in department, course prior ave 3.68)

Spring 2002. Q1 4.0, Q3 4.0, Q4 4.1, Ttl 4.03 (52nd percentile in department)

Spring 2003. Q1 4.34, Q3 4.54, Q4 4.70, Ttl 4.53 (84th percentile in department)

Spring 2004. Q1 4.8, Q3 4.9, Q4 4.9, Ttl 4.87 (99th percentile in department)

Spring 2005. Q1 4.4, Q3 4.7, Q4 4.6, Ttl 4.57 (87th percentile in department)

Spring 2007. Q1 4.53, Q3 4.87, Q4 4.87, Ttl 4.76 (96th percentile in department)

Winter 2008. Q1 4.6, Q3 4.8, Q4 4.8, Ttl 4.73 (92nd percentile in department)

EE 541: Automated Layout of Integrated Systems

Winter 2000. Q1 4.06, Q3 4.67, Q4 4.67, Ttl 4.47 (86th percentile in department, first recent offering)

Winter 2001. Q1 4.58, Q3 4.89, Q4 4.89, Ttl 4.78 (98th percentile in department)

Winter 2002. Q1 4.65, Q3 4.84, Q4 4.81, Ttl 4.77 (97th percentile in department)

Winter 2003. Q1 4.53, Q3 4.78, Q4 4.72, Ttl 4.68 (93rd percentile in department)

Winter 2004. Q1 4.8, Q3 4.9, Q4 4.9, Ttl 4.87 (99th percentile in department)

Winter 2005. Q1 4.3, Q3 4.4, Q4 4.7, Ttl 4.47 (83rd percentile in department)

Winter 2007. Q1 4.3, Q3 5.0, Q4 4.9, Ttl 4.7 (92nd percentile in department)

Winter 2008. Q1 4.4, Q3 4.8, Q4 4.6, Ttl 4.6 (87th percentile in department)

Northwestern (Course prior average is the average instructor ranking for the previous 2-3 years for that course)

B01: Introduction to Digital Logic Design

Winter 1997. CTEC 5.0/6.0 (62nd percentile in department, course prior average 36th percentile)

Fall 1997. CTEC 5.6/6.0 (95th percentile in department)

Fall 1998. CTEC 5.5/6.0 (90th percentile in department)

C11: Data Structures and Data Management

Winter 1996. CTEC 3.4/4.0 (70th percentile in department, course prior average 39th percentile)

C55: Computer Architecture I

Fall 1996. CTEC 5.6/6.0 (95th percentile in department, course prior average 57th percentile)

C91: VLSI Systems Design

Spring 1996. CTEC 3.8/4.0 (97th percentile in department, course prior average 70th percentile)

Spring 1997. CTEC 5.6/6.0 (95th percentile in department)

Winter 1998. CTEC 5.4/6.0 (86th percentile in department)

Winter 1999. CTEC 5.1/6.0 (66th percentile in department)

C92: VLSI Systems Design Projects

Spring 1998. CTEC 5.0/6.0 (62nd percentile in department, first offering of course)

Spring 1999. CTEC 5.5/6.0 (90th percentile in department)

Northwestern Advisor Rating: 1996-1997 4.0/4.0 (Department average 3.2/4.0)

Student Supervision

Graduate Students Supervised

Morgan Enos, M.S., "Replication for Logic Partitioning", September 1996.

Oliver Stone, M.S., "A Comparison of ASIC Implementation Alternatives", October 1996.

Matt Hosler, M.S., "High-Performance Carry Chains for FPGAs", October 1997.

Guangyu Gu, M.S., "Accelerating Photoshop Applications with Reconfigurable Hardware", May 1999.

Venkatesh Karnam, M.S., "Applications of Reconfigurable Logic", March 2000.

Thomas Fry, M.S., "Hyperspectral Image Compression on Reconfigurable Platforms", June 2001.

Melany Richmond, M.S., "A Lemple-Ziv based Configuration Management Architecture for Reconfigurable Computing", July 2001.

Chandra Mulpuri, M.S., "Runtime and Quality Tradeoffs in FPGA Placement and Routing", July 2001.

Zhiyuan Li, Ph.D., "Configuration Management for Reconfigurable Systems", November 2001.

Katherine Compton, M.S., "Programming Architectures for Run-Time Reconfigurable Systems", Fall 1999. Ph.D. "Architecture Generation of Customized Reconfigurable Hardware", September 2003.

Mark Chang, M.S., "Adaptive Computing in NASA Multi-Spectral Image Processing", Fall 1999. Ph.D. "Variable-Precision Analysis for FPGA Synthesis", July 2004.

Shawn Phillips, M.S., "Layout Generation for Application-Specific FPGAs", July 2001. Ph.D. "Automatic Layout of Customized Reconfigurable Hardware", October 2004.

Akshay Sharma, M.S., "Mapping Algorithms for Application-Specific FPGAs", December 2001. Ph.D. "Place and Route Techniques for FPGA Architecture Advancement", Spring 2005.

Mark Holland, M.S. "FPGAs in Computer Architecture Education" May 2002. Ph.D. "Automatic Creation of Product-Term Based Reconfigurable Architectures for System-on-a-Chip", Summer 2005.

Ken Eguro, M.S. "Encryption-Specific FPGA Architectures", Fall 2002. Ph.D. expected 2008.

Todd Owen, M.S. "FPGA Implementation of Error Correction and Improved SPIHT Compression for NASA Hyperspectral Images", June 2003.

Kimberly Motonaga, M.S. "Encryption RaPiD: A Comparison of Custom and Standard-Cell Designs", December 2003.

Brigette Huang, M.S. "Generation of Domain-Specific 2D FPGA Architectures", Winter 2004.

Michael Haselman, M.S. "Bitwidth Analysis of Floating-Point Computations for FPGA Implementations", Spring 2005. Ph.D. expected 2008.

Michael Beauchamp, M.S. "FPGA Architectural Support for Floating Point Computations", Summer 2006.

Peter Grossman, M.S. "Benchmarking Independence on the Triptych Architecture", Fall 2006.

Don DeWitt, M.S. "An FPGA Implementation of Statistical Based Positioning for Positron Emission Tomography", June 2008.

Nikhil Subramanian, M.S. expected Spring 2009.

Brian Van Essen, Ph.D. "Power-Efficient Coarse-Grained FPGA Architectures", expected Spring 2009.

Jimmy Xu, M.S. expected Spring 2010.

Stephen Friedman, Ph.D. expected Spring 2010.

Aaron Wood, Ph.D. expected Spring 2010.

Robin Panda, Ph.D. expected Spring 2010.

Allan Carroll, M.S. expected Summer 2008. Ph.D. expected 2011.

Undergraduate Student Projects Supervised

John Seng, "High-Speed Placement for Logic Emulation Systems", Spring 1996.

Emmett Tomai, "The Trichromic Board: Reconfigurable Video Processing", Spring 1996 - Winter 1997.

Thomas Fry, "Chimaera: Design of a Reconfigurable Functional Unit", Summer 1996 - Spring 1998.

Jeff Kao, "VLSI Implementation of the Chimaera Reconfigurable Functional Unit", Fall 1996 - Spring 1997.

Michael Malitsky, Felix Nayman, Yan Pechenik, Mike Yamnitsky, "Design Competition, Team: Abort, Retry, Fail; Robot: Red October", Fall 1996 - Spring 1997.

Katherine Compton, Honors Project, "Mapping Methods for the Chimaera Reconfigurable Functional Unit", Winter 1997 - Fall 1997.

Stephen Knol, "Data Security for Web-based CAD", Spring 1997 - Winter 1998; Honors Project, "Logic Restructuring for Logic Partitioning", Spring 1998 - Winter 1999; "Harnessing FPGA logic for Communication Protocols", Winter 1999 - Spring 1999.

Vernell Chapman, "Web-based Distributed Computing Infrastructure", Summer 1997 - Fall 1997.

Dennis Kiilerich, "Software Support for the Chimaera RFU", Fall 1997.

Doug Wilson, "Applications of Reconfigurable Hardware", Fall 1997 - Spring 1998; Honors Project, "Configuration Compression Techniques for Reconfigurable Computing", Summer 1998 - Fall 1998.

Jason Gonzalez, Tilman Gruber, "Design Competition, Team: Autobot", Fall 1997 - Spring 1998.

Matt Wuebbing, "Applications of the Chimaera RFU", Spring 1998.

Jake Brick, "Image Expansion Using Reconfigurable Logic", Fall 1998 - Winter 1999.

Shirley Chan, "Color Space Conversion Using Reconfigurable Logic", Fall 1998 - Spring 1999.

Ken Eguro, Honors Project, "Wavelet Compression of Image Data Using Reconfigurable Logic", Fall 1998 - Spring 1999.

Mayank Gupta, "Fast Place & Route for Xilinx FPGAs", Fall 1998 - Winter 1999.

Rajeev Krishna, "VLSI Chip Testing: MacTester, Logic Emulator", Fall 1998 - Spring 1999.

Paymon Farazi, "Applications of the Chimaera RFU", Winter 1999 - Spring 1999.

Nitin Jain, "Implementation of SPIHT Compression in FPGAs", Winter 2000 - Fall 2000.

Tim Midgett, "Instruction-set design for FPGA-based Computer Architecture Education", Fall 2000 - Winter 2001.

James Harris, "Instruction-set design for FPGA-based Computer Architecture Education", Fall 2000 - Spring 2001.

Jason Long, "AES Encryption on Xilinx FPGAs", Summer 2001.

Theresa Le, "AES Encryption on Xilinx FPGAs", Summer 2001.

Ouail Albairat, "AES Encryption on Xilinx FPGAs", Summer 2001 – Summer 2002.

Steve Detmer, "Implementation of a MIPS processor on an FPGA", Fall 2001.

Kevin Curtiss, "DSP Algorithms on the RaPiD System", Spring 2002.

Ben Medina, "Encryption Algorithms on the RaPiD System", Spring 2002.

Seung Chung, "Verilog Implementation of AES Encryption Algorithms", Spring 2002 – Fall 2002.

Angus MacDuffie, "Image Processing Algorithms on the RaPiD System", Summer 2001 - Spring 2003.

Michael Beauchamp, "Encryption Algorithms on the RaPiD System", Spring 2002 – Spring 2003.

Michael Haselman, "Encryption Algorithms on the RaPiD System", Spring 2002 – Spring 2003.

Alexander Pasciak, "Verilog Implementation of AES Encryption Algorithms", Spring 2002 – Spring 2003.

Bruce Lam, "Layout of the Encryption RaPiD Chip", Fall 2002 – Spring 2003.

Stephen Freeman, "FPGA Applications for LLNL", Fall 2002 – Spring 2003.

Jason G. Louie, "Encryption Algorithms on the RaPiD System", Winter 2003 – Spring 2003.

Daniel Hartono, "Layout of the Encryption RaPiD Chip", Winter 2003 – Spring 2003.

Benjamin Byer, "Layout of the Encryption RaPiD Chip", Winter 2003 – Spring 2003.

Allen Berg, "DSP Algorithms on the RaPiD System", Spring 2002 – Summer 2003.

Gwyneth Hoi Shan Chan, "Encryption Algorithms on the RaPiD System", Winter 2003 – Summer 2003.

Clara Lo, "Layout of the Encryption RaPiD Chip", Winter 2003 – Summer 2003.

Nick Sherman, "Layout of the Encryption RaPiD Chip", Winter 2003 – Summer 2003.

Jung E. Kim, "Verilog Implementations of European & Japanese Encryption Algorithms", Spring 2003 – Summer 2003.

Daniel Scott Hippe, "Verilog Implementations of European & Japanese Encryption Algorithms", Spring 2003 – Summer 2003.

Eka Purnama Tjung, "Verilog Implementations of European & Japanese Encryption Algorithms", Spring 2003 – Summer 2003.

David Harold Dailey, "Verilog Implementations of European & Japanese Encryption Algorithms", Spring 2003 – Summer 2003.

Henry Lee, "Verilog Implementations of European & Japanese Encryption Algorithms", Spring 2003 - Summer 2003. "FPGA Support for Floating-Point Computations", Fall 2003 – Spring 2004.

Aaron Wood, "FPGA Support for Floating-Point Computations", Fall 2003 – Spring 2004, Fall 2004; College Honors Thesis, "The Implications of Floating Point Computations on FPGAs", Winter 2005 – Spring 2005.

Patrick McMurchie, "Enhancements to the Independence Placer", Fall 2004 – Winter 2005.

Jenny Bui, "Simulated Annealing Placement for the Triptych FPGA", Winter 2005 – Spring 2005.

Jason Wong, "Retargetting Independence to the Triptych FPGA", Winter 2005 – Spring 2005.

Courtney Wands, "VLSI Demonstrations for Educational Outreach", Winter 2007 – Spring 2007.

Christine Steele, "VLSI Demonstrations for Educational Outreach", Winter 2007 - Spring 2007.

Kristofer Plunkett, “Macah Implementations of K-Means Clustering”, Spring 2007.

Brian Mayton, “Macah Implementations of PCA”, Spring 2007.

Elliott Conant, “Macah Implementations of FFTs”, Spring 2007 – Summer 2007.

Nick Hunt, “Macah Implementations of FFTs”, Autumn 2007.

Jon Andes, “Macah Implementations of Signal Processing Algorithms”, Autumn 2007.

Jordan Hoyt, “Macah Implementations of PCA”, Spring 2007 – Spring 2008.

Ben Weintraub, Honors Project, “Accelerating bioinformatics algorithms on micro-parallel architectures”, Spring 2007 – Spring 2008.

Robert Horrox, “VLSI Demonstrations for Educational Outreach”, Autumn 2007 – Winter 2008.

Jimmy Xu, VLSI Demonstrations for Educational Outreach”, Autumn 2007 – Spring 2008.

Yuhong Wang, “Macah Implementations of Signal Processing Algorithms”, Spring 2008.

Chad Jerde, “Ambric Implementations of a PET Scanner”, Spring 2008.

Maria Kim, “Ambric Implementations of a PET Scanner”, Spring 2008.

Danny Anderson, Honors Project, “Macah Implementations of Signal Processing Algorithms”, Spring 2008.
