# Low Latency Edge Classification GNN for Particle Trajectory Tracking on FPGAs

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Abstract—In-time particle trajectory reconstruction in the Large Hadron Collider is challenging due to the high collision rate and numerous particle hits. Using GNN (Graph Neural Network) on FPGA has enabled superior accuracy with flexible trajectory classification. However, existing GNN architectures have inefficient resource usage and insufficient parallelism for edge classification. This paper introduces a resource-efficient GNN architecture on FPGAs for low latency particle tracking. The modular architecture facilitates design scalability to support large graphs. Leveraging the geometric properties of hit detectors further reduces graph complexity and resource usage. Our results on Xilinx UltraScale+ VU9P demonstrate 1625x and 1574x performance improvement over CPU and GPU respectively.

## I. INTRODUCTION

Particle trajectory reconstruction in Large Hadron Collider (LHC) is a vital task for collision analysis, which requires accurate and in-time reconstruction to decide which collision events to read out [1]. The existing reconstruction algorithms are based on Kalman filter [2], [3], [4], [5], which are difficult to meet strict latency requirements due to the quadratically increasing complexity. The High-Luminosity LHC project [6], [7] aims to boost the instantaneous luminosity by 5x to 7x in 2027, even exacerbating the design challenges for trajectory reconstruction. Recent research shows that edge-classifying GNNs (Graph Neural Networks) achieve high accuracy in trajectory reconstruction and are scalable with the increased luminosity [8], [9], [10], [11], [12], [13], making them a preferred solution for future collision analysis in LHC.

One of the main concerns for GNNs to be implemented in the LHC system is the long processing latency with irregular data accesses. Recently proposed GNN accelerators [14], [15], [16], [17], [18], [19] are designed to focus on node data, such as Graph Convolutional Networks (GCNs) [20] and GraphSAGE [21]. These cannot be applied directly to the edge classifying GNNs in trajectory reconstruction, which uses edge embedding and predicts the results on edges. Moreover, preprocessing on graphs is not fit for trajectory reconstruction which has relatively smaller but dynamic graph properties. State-of-the-art accelerators optimize their performance by reducing irregularity, such as rearranging processing patterns and order to better fit with their architectures [15], [19], or monitor the utilization of processing elements (PEs) to balance the workload [17]. These techniques are beneficial for static and large graphs, where stable graph characteristics can be reused. However, it is not efficient to spend long preprocessing time for one-time use on small graphs with dynamic features.

In this paper, we propose an efficient architecture on FPGAs to support edge-classifying GNNs, meeting the timing requirement of LHC tasks. There are three novel contributions in the proposed architecture. First, a modular parallel architecture facilitates the design and scaling of the architecture with the size of the graphs. Second, efficient data allocation and buffer arrays considerably reduce memory conflicts during parallel data accesses. Third, exploitation of the geometry of collision events significantly lowers the graph irregularity by constraining the node connections, and thus increases processing parallelism.

This work is implemented with the high-level-synthesis framework, hls4ml [22], [23], which enables an automatic translation of machine learning models to FPGA designs. The experiments were performed on real collision graphs. The results on a Xilinx Virtex UltraScale+ VU9P FPGA show that the proposed GNN architecture achieves 1,625x and 1,574x speedup respectively compared with a Intel Xeon W-2125 CPU and an NVIDIA RTX2080 GPU. Section II of this paper discusses the background of particle tracking. Section III introduces the proposed GNN architecture. Section IV evaluates the performance and Section V concludes this work.

#### II. BACKGROUND

## A. Large Hadron Collider System

The Large Hadron Collider (LHC) is the largest and most powerful particle accelerator in the world [6]. For high-energy particle physics collider experiments in the LHC, protonproton collisions occur at a frequency of 40MHz and produce data at a rate of roughly 40 TB/s [1]. After the collision, the trackers record the locations of particle detections ("hits") and transfer this information to the trigger systems. The trigger system will perform trajectory reconstruction to recognize which hits belong to the same particle, as shown in Fig. 1. The collision events are processed by 18 FPGAs in a multiplexed manner, where each FPGA needs to handle 2.22 million graphs per second (MGPS) [24].

Trackers are composed of cylindrical detecting layers [6], [13]. These layers are immersed in an axis-aligned magnetic field, and their geometry is naturally described by cylindrical coordinates. We focus on the innermost layers, a highly granular set of 4 barrel and 14 endcap layers [25].



Fig. 1: Illustration of trajectory reconstruction

#### B. GNN-based Algorithms for Track Reconstruction

The edge classifying GNN algorithm is based on interaction networks (IN) [26]. IN is a physics-motivated GNN capable of analyzing objects and their relations. Hit information is embedded in the node feature, and trajectory segment information is embedded in the edge feature. The index set stores the sender and receiver node indexes of each edge. There are three types of functions in IN: Edgeblock, Aggregate, and Nodeblock. Functions in Edgeblock and Nodeblock are multi-layer perceptrons (MLPs) that re-embed edge and node features according to their input. Aggregate accumulates edge features to their receiver nodes.

## C. Designs of GNN Accelerators on FPGAs

Several studies have implemented GNNs on FPGAs for particle physics [8], [25], [27]. [8] focuses on jet tagging, which targets fully connected graphs and aims to predict features of the entire graph instead of each individual edge. While [8] addresses the issue of irregular access with fully connected graph properties, it is not suitable for the LHC application. The graphs generated from the LHC consist of hundreds of nodes per graph. Utilizing the methods from [8] may generate excessive unnecessary connections which may be tens to hundreds of times greater than the original graph, leading to a significant impact on processing time.

# III. A LOW LATENCY GNN ARCHITECTURE FOR TRAJECTORY RECONSTRUCTION

#### A. Overview Architecture

Based on the GNN computation flow of IN in Section II-B, the computation can be split into pipeline stages at the function level. We use the Vivado HLS dataflow architecture to implement the pipeline. Fig. 2a shows the proposed pipeline. We design a modularized parallel architecture for each function, including Edgeblock, Aggregate and Nodeblock. Each function is composed of several processing elements (PEs) as basic compute units. Between these functions, we insert FIFO

buffers with different depths to ensure that data would not be stuck in the dataflow paths. With this architecture, users can configure the pipeline and scale the system throughput with the available resources on FPGAs.

#### B. Modular Parallel Architecture

The modular parallel architecture enables parallel processing of each function. The following introduces the design and optimizations of these functions.

1) Edgeblock: The Edgeblock computation involves accessing edge features, edge indexes, and connected node features. The access of node features changes dynamically according to the edge indexes. To address this irregularity, we added node arrays, which contain the features of all the nodes in the graph, into each PE to support concurrent accesses to node features. As shown in Fig. 2b, during the computation, the edge features  $(e_{i,j})$  and edge indexes (i, j) of each edge will be sent to PEs. In each PE, node features  $(X_i \text{ and } X_j)$  are accessed based on the edge indexes. After the above steps, multiplier engines in PEs will process the MLP computation and output the updated edge features.

2) Aggregate: The purpose of Aggregate is to send the updated edge features to their receiver nodes. During this process, the aggregate function first reads updated edge features and edge indexes. Based on the edge indexes, the aggregated edge features are accessed and added to the updated edge features, and then stored back to internal registers. The architecture of Aggregate PE is shown in Fig. 2c. After aggregating all updated edge features, the parallel adder tree accumulates the values of the same node indexes. With this architecture, multiple Aggregate PEs can process multiple edges simultaneously.

3) Nodeblock: The Nodeblock is used for re-embedding node features by the original and aggregated node features. The data access of the Nodeblock computation is more regular when compared with Edgeblock and Aggregate. For each node, Nodeblock collects node features and aggregated node features, and then uses MLPs to obtain updated node features.

## C. Exploiting Geometric Property of LHC Trackers

While the architecture in the previous section successfully enables significant parallelism between processing elements (PEs), the individual memory in PEs costs considerable amount of BlockRAMs (BRAM) in an FPGA. Therefore, we propose a method that can reduce memory utilization and enable a more parallel architecture by taking advantage of the data properties of LHC detectors.

In Section II-A, we introduced the architecture of the LHC particle trackers and how hit data is applied to the input graphs of GNNs. In the original graph constructed from LHC trackers, an edge from a node could connect to any other node in a graph. This assumption could cause excessive number of edges in the graph. Since the LHC trackers are composed of cylindrical layers surrounding the colliding beams, the particles have to pass through the inner tracker layer first and then move out, as shown in Fig. 3a. These trajectories exhibit similar connection behaviors. For example, hits on the B1 layer



Fig. 2: (a) Overview architecture of the system processing block. (b) An architecture of Edgeblock with two PEs. (c) The architecture of Aggregate with two FEs

only connect to the B2 layer or E1 layer. The relationship between hits and legal edges can be applied to a geometryconstrained graph. We reorganize the input graph structure by grouping hits based on their layer locations. We partition the graphs into 13 parallel sub-graphs, each containing only two node groups, as shown in Fig. 3b and 3c.



Fig. 3: (a) Possible trajectories of particles, (b) Partition layers into two types of node group (c) Partition a graph into subgraphs

With the geometry-constrained approach, an edge can only exist between specific node groups. This reduces the number of candidate nodes in node arrays used in Edgeblock PEs and Aggregate PEs, resulting in significant reduction of memory usage. Furthermore, since these 13 sub-graphs are independent of each other, they can be assigned to different PEs and computed in parallel. By relieving memory usage pressure and improving parallelism, the performance is greatly enhanced compared to the original design.

# IV. EVALUATION

# A. Experiment Setup

We implemented our design with Vivado HLS 2019.2 and loaded it onto a Xilinx Virtex UltraScale+ VU9P FPGA. The clock frequency of the design runs at 200 MHz. The resource utilization is from the v-synthesis report. The performance is based on the simulation result of the generated HDL code. We use the metric of Million Graphs Per Second (MGPS) to measure the system throughput.

We evaluate our architecture with the TrackML dataset [28] generated by CERN. All the data points are based on a fixed point format of 7 integer bits and 7 fractional bits. This is the same format used in [25] to ensure acceptable accuracy.

A system PE in the experiment contains an Edgeblock PE, an Aggregate PE, and a Nodeblock PE. The graph size of the dataset will be elaborated in Section IV-B. The performance of our proposed architecture will be evaluated in Sections IV-C to IV-E. In Section IV-F, we compare the performance of our architecture with the CPU, GPU, and prior FPGA designs.

# B. Supporting In-time Graph Processing of Collision Events

The ultimate goal of this work is to perform in-time trajectory reconstruction based on the graphs generated from LHC collision events. Input graphs are prepared based on the same flow as the prior work [25]. Each graph is divided into two sectors based on the position z of hits. We use the graph size that can cover 95 percentile of collision events as the nominal size, which contains 739 nodes with 1252 edges. According to [24], these graphs should be computed at the throughput higher than 2.22 MGPS.

Table I compares the three proposed architectures. The architecture MPA represents the Modular Parallel Architecture introduced in Section III-B. MPA<sub>geo</sub> and MPA<sub>geo\_rsrc</sub> are the extended designs of MPA with the proposed techniques of geometry-constrained optimization and data-aware resource allocation respectively. The designs of MPA<sub>geo</sub> and MPA<sub>geo\_rsrc</sub> will be elaborated in Section IV-D and IV-E. Latency measures the time from input graph to the output result. The design can take a new input in every Interval time and attain throughput in MGPS. As shown in Table I, the proposed MPA<sub>geo\_rsrc</sub> meets the LHC requirement by supporting graphs of 739 nodes with 1252 edges at throughput of 3.225 MGPS.

TABLE I: Performance of the proposed architectures

Architectures	Latency( $\mu$ s)	Interval( $\mu$ s)	Throughput(MGPS)
MPA	3.165	0.48	2.083
MPAgeo	2.69	0.425	2.352
MPAgeo_rsrc	2.07	0.31	3.225

# C. Scalability of MPA (Modular Parallel Architecture)

In Section III-B, we introduced the MPA architecture. The processing throughput of the architecture can scale by deploying more PEs. To evaluate the scalability of MPA, Fig. 4 illustrates the performance and resource utilization of MPA from one PE to eight PEs. The results show the latency and interval can be reduced by deploying more PEs. However, when scaling up the number of PEs, BRAMs will become the limiting factor of FPGA resources.



Fig. 4: Scalability of the modular architecture

#### D. MPA with Geometry-constrained Optimization

By taking advantage of the geometry-constrained property described in Section III-C,  $MPA_{geo}$  not only relieves the constraints of the range of node in each PE, but also makes node groups independent to others.  $MPA_{geo}$  alleviates the resource demand of BRAM and allows the deployment of more PEs for greater processing parallelism. There are 11 node groups and 13 edge groups. We allocate one PE for each of these groups and result in a total of 11 Nodeblock PEs, 13 Edgeblock PEs, and 13 Aggregate PEs. As shown in Table I,  $MPA_{geo}$  achieves 13% improvement in throughput compared to the original MPA architecture.

## E. Data-aware Resource Allocation

We further analyze the distribution of graph sizes in the dataset and propose the design MPA<sub>geo\_rsrc</sub> which applies data-aware resource allocation. After applying the geometry-constrained property, the number of nodes are not evenly distributed across different layers. The barrel layers (B1 to B4) contain more nodes and connections than endcap layers (E1 to E7). To address this issue, we propose the design MPA<sub>geo\_rsrc</sub> which classifies the node groups into two types. As shown in Fig. 3b, the layers B1 to B4 contain relatively more nodes and belong to type A, while layers E1 to E7 with fewer nodes are assigned to type B. We will assign two PEs to process each node group of type A, and one PE to handle each node group in type B. For the edge groups, we apply the same allocation principle as for node groups.

TABLE II: Allocate PEs based on different sizes of data

	No	de		Edge	
	Α	В	A-A	A-B	B-B
#data	138	62	277	77	87
#PE	2	1	4	1	1

#### F. Comparison with Previous Designs

1) Comparison with Previous GNN Trajectory Reconstruction on FPGA: There are two architectures in the previous

work [25] of GNN for trajectory reconstruction on FPGA. The throughput-optimized design (ThrpOpt) focuses on attaining high throughput, but would reduce the graph size it can handle. The resource-optimized design (RsrcOpt) aims to accommodate large graphs, but would suffer from low throughput. Table III compares the performance between these two architectures and our proposed architecture. The platform of all the three architectures is XCVU9P, and the frequency is 200 MHz. ThrpOpt design can achieve a higher throughput of 200 MGPS, but can only handle small graphs of 28 nodes with 56 edges. RsrcOpt architecture can accommodate large graphs of 448 nodes with 896 edges, but with lower throughput than the ThrpOpt design. Our proposed MPAgeo resrc can handle the largest graph (739 nodes with 1252 edges) among all the designs, and attains higher throughput than the RsrcOpt design.

TABLE III: Comparison with previous FPGA designs

	ThrpOpt [25]	RsrcOpt [25]	MPAgeo_rsrc (proposed)
Graph Size	28 nodes/56 edges	448 nodes/896 edges	739 nodes/1252 edges
Throughput	200 MGPS	1.14 MGPS	3.17 MGPS

2) Comparison with CPU and GPU: We execute the same particle-tracking GNN algorithm on an Intel(R)Xeon(R) W-2125 CPU and an NVIDIA GeForce RTX 2080 Ti (CUDA 10.2) based on PyTorch (1.11.0) and the PyTorch Geometric 2.0.4 framework. We ran 1000 graphs on each platform. Each graph contains 739 nodes and 1252 edges. Table IV shows the details of experiment and normalized throughput. Our proposed design on FPGA achieved significantly higher throughput of 1,625x and 1,574x when compared with CPU and GPU respectively.

TABLE IV: Comparison with CPU and GPU

	CPU	GPU	FPGA
Platform	Intel(R) Xeon(R)	NVIDIA GeForce	XCVU9P
	W-2125	RTX 2080 Ti	
Compute Unit	4.00 GHz@8 cores	1.63 GHz@4352 cores	200 MHz
Technology	14 nm	12 nm	14 nm
Normalized Thrp.	1	1.03	1625

#### V. CONCLUSION

We propose a novel architecture for particle-tracking GNNs on FPGAs. By utilizing LHC detector geometry, our design reduces graph complexity and FPGA resource requirements. The modular architecture of processing units and buffers also efficiently handle the irregular data access patterns and facilitate design scalability to support large graphs while attaining high parallelism and computation throughput. Experiment results show that our design achieves 1,625x speedup compared to the CPU, and 1,574x speedup compared to the GPU.

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