

Vaibhav Vaidya

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7844, 14th Ave NE
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98115 (*until 07/2007*)

OBJECTIVE Intern position for a challenging experience in Analog Circuits research

EDUCATION

University of Washington, Seattle

PhD in Electrical Engineering (approx. Autumn 2008) September 2005 – Present

- **Research – Organic Electronics: Modeling and Circuits (Prof. Denise Wilson)**
- **Present GPA 3.88**
- **Graduate level Classes in Analog RF, PLLs, Digital VLSI, ADCs, DSP, MEMS**

Goa Engineering College, India

Bachelor of Electronics and Telecommunication Engineering July 1999 – June 2003

- **Graduated with First Class, Honors**

Research

- **Reconfigurable Computing with a PCI-Bus based multi-FPGA Testbed**
 - Hardware: VHDL design for PCI I/O, Reconfigurable Computing Control, Test Designs (verification)
 - Software: 5Mbps PCI driver on Linux, User API, FPGA Configuration/Reconfiguration

WORK EXPERIENCE

Intel Corporation

Graduate Intern *at Dupont (Washington)* Summer 2006

- **PCIE (gen2)** : Transmitter Circuits performance evaluation, circuit design issues

Graduate Intern *at Ronler Acres, Hillsboro (Oregon)* Summer 2005

- **Cache Circuits** : Investigating techniques for dynamic performance control of Level-1 Cache Memory
Performance estimation, Bias circuit design, Integration with production models of L1 Cache

National Institute of Oceanography

Project Trainee *at Goa, India* Summer 2004

- Built a **Data Acquisition System for a ship-board echo-sounder**: Hardware interface and Device Driver (for a 100ksps card in Linux) to capture the Analog Echo signal, User Programs to preprocess and make it amenable for Neural characterization systems for the classification of Sea Bottom

TOOLS

- EDA:- *VHDL / Verilog, Xilinx ISE, ModelSim, Hspice, Pspice, Cadence, Synopsys*
- Programming:- *Java, C – Linux, Perl*

CLASSES

- **Analog RF Design** – Schematic design of a 2.4GHz down-converter (IBM 0.18 μ m)
- **PLLs** – Schematic design of an Integer-N PLL for frequency synthesis (IBM 0.18 μ m)
- **ADCs** – Non-credit (Spring 2007)
- **Digital Design** – Schematic design of a 256 bit SRAM; Schematic, Layout of a Standard Cell Library (TSMC 0.18 μ m)
- **Special Circuits** – Schematic design of a 'Winner-Take-All' circuit based A/D converter (AMI 1.5 μ m)

REFERENCES

Available on Request