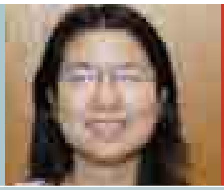

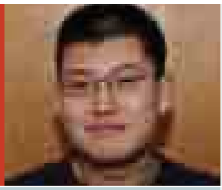

Signal Integrity in 3D High-Speed Interconnects

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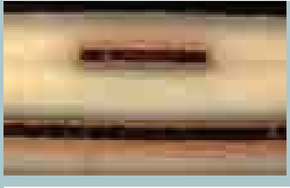
Signal integrity affects all levels of microelectronics packaging for high-speed circuits. Signal integrity research attempts to identify and avoid any effect that causes signal distortion and energy loss at high frequency range. Signaling rates are expected to exceed 10 Gb/s in a few years, which makes it important to understand off-chip loss due to metal surface roughness. Another issue is the multiple scatterings among the vertical via structures in the multi-layer dielectric substrate. Ever-increasing edge rates will raise the likelihood of cross-talk, ground bounce, resonance, attenuation and other signal discontinuities among squeezed signal lines. These are important issues for high speed circuit design and modeling.

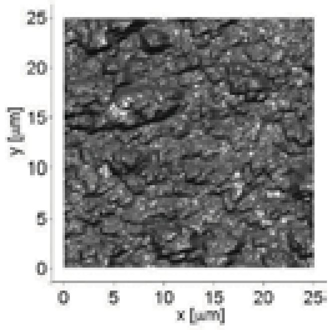
To model the surface-roughness effect of the signal integrity in interconnects on high-speed packages and board, the rough surface is characterized by a stochastic process with spectral density function. From 3D roughness profiles of atomic force microscope (AFM) measurements, the spectral densities were extracted. We considered the problem of a plane wave incident on a rough dielectric-metal surface and also the problem of a source in a metallic waveguide with a rough interface. To solve Maxwell equations for the problem, the analytic small perturbation method and numerical methods were used (the Method of Moments (MoM) and the transfer operator matrix (T-Matrix)).

For multiple vias scattering problem, this method consists of a full wave 3D characterization using the MoM with layered media Green's functions for the exterior microstrip-to-via problem, and the Foldy-Lax multiple scattering equations for the interior vias between the reference planes. The semi-analytic formulations model the vias by using waveguide modes in the vertical direction, and cylindrical wave expansions in the horizontal direction. The layered medium Green's functions are generated rapidly, using fast all modes method (FAM) and numerical modified steepest-descent path method (NMSP). These methods solve the complicated interconnecting structures many times faster than the available commercial software.

Simulation shows that a rough surface interface can cause up to 100% more power loss than a smooth surface interface. The Via-Foldy-Lax simulation tool provides multi-port network parameters several thousand times faster than the commercial software (HFSS). The 3D full wave method is now being extended to more complicated configurations such as 3D waveguide roughness and multi-layered stacked problems. eeKO8

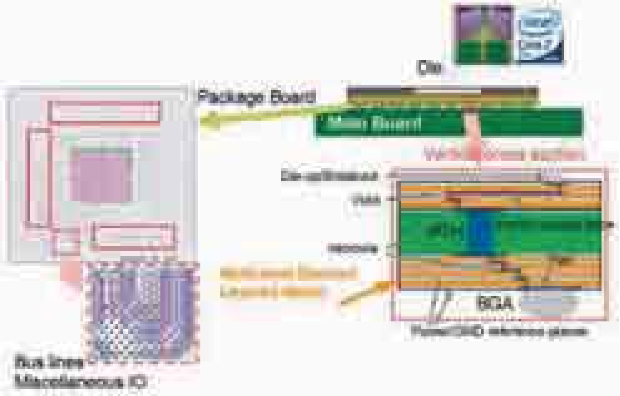


A side view of the rough interface between the printed transmission line and the substrate, taken at the polished cross-section.



A top view of the rough interface between the printed transmission line and the substrate taken by the atomic force microscope.

Below: Multi-layer stacked vias in the IC package.



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