Symbolic Analysis of Analog Circuits with Hard Nonlinearity*

Alicia Manthe, Zhao Li, and C.-J. Richard Shi
Department of Electrical Engineering, University of Washington, Seattle, WA 98195
{amanthe, lz2000, cjshi}@ee.washington.edu

ABSTRACT

A new methodology is presented to solve a strongly nonlinear circuit, characterized by Piece-Wise Linear (PWL) functions, symbolically and explicitly in terms of its circuit parameters and is amenable to computer implementation. The method is based on a modified nodal formulation of piecewise linear circuit equations as a *mixed* Linear Complementarity Problem (MLCP). The technique of determinant-decision diagrams is applied to implement the symbolic transformation of the MLCP to the standard LCP. Complementarity-decision diagrams are used to represent the resulting LCP. Examples are presented that demonstrate the accuracy and efficiency of the proposed method.

Categories and Subject Descriptors

T5.3 Analog and mixed-signal design tools and RF

General Terms Algorithms

Keywords

Symbolic Analysis, Circuit Nonlinearity, PWL

1. INTRODUCTION

Analysis of the effect of device nonlinearity on the system performance is critical to high-performance analog/RF systems-on-chip design [5][8]. While a class of nonlinear circuits, known as *weakly nonlinear,* can be analyzed via linearized techniques such as small-signal analysis or techniques based on linearized analysis such as harmonic balance or Volterra series [10], many circuits ranging from switches, mixers, saturation-limited amplifiers to switched-capacitor filters and switching power converters, exhibit strong nonlinearities. Circuits exhibiting strong nonlinearities refer to sudden changes of device behavior, for example, switching of operating regions, sudden changes of device physics, and piecewise I-V characteristics.

Strong nonlinearities also arise in the following two scenarios. First, there is increasing interest in using digital logic signals to control the operations of analog/RF front-ends. As a consequence, more "novel" analog signal processing circuits may change their behaviors abruptly. Second, with the analog hardware description languages such as VHDL-AMS and Verilog-AMS gaining more momentum [5], behavioral models are being developed for systems-on-chip simulation and architecture evaluation. Many behavioral models are characterized as piecewise linear models consisting of sudden behavior changes.

Analysis of circuits demonstrating strong nonlinearities is known to be challenging [8]. Time-varying Volterra series [12], sliding kernels dynamic Volterra series [3], and describing functions [4] have been proposed to handle a certain class of circuits such as mixers, the methods depend highly on the specific circuit structure, require derivatives, and are hard to automate. Further, the complexity increases dramatically when high order series are required. The multi-rate partial differential equation (MPDE) formulation [10] can compute numerically the multi-rate behavior efficiently with strong known linearity such as output spikes. However, the method also requires the computation of a Jacobian matrix, which prohibits its use towards hard nonlinearity analysis.

This paper presents a new method capable of analyzing explicitly and exactly the behavior of circuits with strong nonlinearities characterized by piecewise linear functions. Our work is inspired by the recent work of Bokhoven and Leenaerts [7], which demonstrates that explicit formulae can be derived for a class of PWL circuits that can be formulated as so-called P-class linear complementarity problem (LCP). Our novel contributions are as follows: (1) To be amenable to computer implementation, we first present a formulation of PWL circuits equations using the framework of Modified Nodal Analysis (MNA). This leads to a mathematical problem known as the Mixed Linear Complementarity Problem (MLCP) [2]. (2) We exploit a compact data structure known as determinant decision diagrams (DDDs) [11] to represent all the manipulations from MLCP to LCP symbolically and utilize complementarity decision diagrams (CDDs) [8] to characterize the LCP expressions.

The method is amenable to computer implementation. Furthermore, it represents all the solutions (voltages and currents) explicitly in terms of circuit parameters, input sources based on a special mathematical operator = $\lfloor . \rfloor$. The symbolic expressions can help designers to gain insight on how circuit parameters affect the circuit linearity. A very efficient numerical time-domain and harmonic simulator have been implemented based on the repetitive evaluation of the resulting expressions. The simulator can calculate the harmonics and time-domain responses exactly, while the SPICE-like numerical simulators have to invoke various smoothing functions to compute the approximate solutions. As observed in our experiments, how the PWL is smoothed can lead

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to significant changes in the operating point, linear and nonlinear circuit characteristics.

This paper is organized as follows. Section 2 presents preliminary PWL information, which is followed by an MNA formulation of PWL circuits as the mixed linear complementarity problem (LCP). Experimental results are described in Section 4. Section 5 concludes this paper.

2. PRELIMINARY

Piece-Wise Linear (PWL) functions are used to model devices that exhibit strong nonlinearities. Numerous research by Chua [1] and furthered by van Bokhoven and Leenaerts [7] derived functions to represent networks consisting of nonlinear devices in an *explicit* form. For an *explicit* model the output vector can be obtained simply by substituting the input vector into the description. Therefore, these functions can be solved in a fraction of time needed by other models, such as, table look-up or spline function approximation.

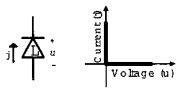


Figure 1. An *orthoator* and its *I-V* curve.

To be able to represent each piece of the PWL function in a behavioral model van Bokhoven and Leenaerts in [7] makes use of an ideal diode. To be amenable to Modified Nodal Analysis (MNA), we will call this "new" basic two-terminal circuit element an *orthoator,* as illustrated in Figure 1. An orthoator describes the behavior of a circuit with "extremely hard" nonlinearities, and it is defined in terms of the current j through the orthoator and the voltage u across the orthoator as

$$u \geq 0, \quad j \geq 0, \quad u^T j = 0. \tag{1}$$

The relationship between u and j is defined as the linear complementarity problem (LCP) [7].

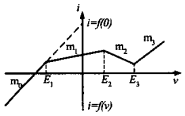


Figure 2: A PWL curve example.

Now consider the one-dimensional continuous PWL function $i = f(v)$ shown in Figure 2. It can be represented by the so-called state-model shown below [7]:

$$i = m^0 v + \begin{bmatrix} b^1 & b^2 & b^3 \end{bmatrix} \mathbf{u} + f(0) \tag{2}$$

$$\mathbf{j} = \begin{bmatrix} -2 \\ -2 \\ -2 \end{bmatrix} v + \mathbf{I}\mathbf{u} + \begin{bmatrix} g^1 \\ g^2 \\ g^3 \end{bmatrix}$$

$$\mathbf{u} \geq 0, \mathbf{j} \geq 0, \mathbf{u}^T \mathbf{j} = 0$$

$$b^k = \frac{m^k - m^{k-1}}{2} \text{ and } g^k = 2 \cdot E^k \text{ for } k = 1 \ldots 3$$

The standard LCP resulting from circuit formulation can be re-written from (2) as follows:

$$\mathbf{u} = \mathbf{D}\mathbf{j} + \mathbf{q} \quad \mathbf{j}^T\mathbf{u} = 0 \quad \mathbf{j}, \mathbf{u} \geq 0 \tag{3}$$

where **u** (voltage across *orthoator*), **j** (current through *orthoator*) and **q** (input sources) are column vectors of size m x 1 and **D** (linear components of the circuit) is a m x m square matrix.

It has been shown that there exists a unique solution to (3) if and only if **D** is of class P, i.e., all the principle minors of the matrix are positive [2]. Then explicit solutions of **j** and **u** can be obtained explicitly using an operator called the modulus transform, which is stated here, as [7]:

$$y = \lfloor x \rfloor \rightarrow \begin{cases} y = x, & x \geq 0 \\ y = 0, & x < 0 \end{cases} \tag{4}$$

and is equivalent to the mapping $u, j \rightarrow z$ which satisfies:

$$|z| = \frac{(u + j)}{2} \text{ and } z = \frac{(u - j)}{2} \tag{5}$$

Consider the 1-dimensional (1-D) case (m = 1). The solution is $u = \lfloor q \rfloor$, $j = 0$ or $j = \lfloor -q/D \rfloor$, $u = 0$. This result is clearly seen by plugging in a zero for u to find j and vice versa.

The solution to the case m = 2 can be broken down to solve the problem of m = 1. Given the 2-D LCP:

$$\begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} D_{11} & D_{12} \\ D_{21} & D_{22} \end{bmatrix} \begin{bmatrix} j_1 \\ j_2 \end{bmatrix} + \begin{bmatrix} q_1 \\ q_2 \end{bmatrix} \tag{6}$$

Assume $j_1 = 0$, then the following is true $u_1 = \lfloor D_{12} * \hat{j}_2 + q_1 \rfloor$ and $\hat{u}_2 = D_{22} * \hat{j}_2 + q_2$. The formulation of $\hat{u}_2$ is equivalent to solving a 1-D case. Assume $\hat{u}_2 = 0$, then $\hat{j}_2 = \lfloor -q_2/D_{22} \rfloor$. Substitute $\hat{j}_2$ into u_1 yields the u_1 expression found in (7). To find j_1 then u_1 must be zero leading to: $0 = D_{11} * j_1 + D_{12} * j_2 + q_1$. Evaluating the function in terms of j_1 leads to the equation found in (7). The solutions for u_2 and j_2 are found the same way and are shown below.

$$u_1 = \left\lfloor D_{12} * \left\lfloor \frac{-q_2}{D_{22}} \right\rfloor + q_1 \right\rfloor \qquad j_1 = \left\lfloor \frac{-D_{12}}{D_{11}} * \left\lfloor \frac{-q_2}{D_{22}} \right\rfloor - \frac{q_1}{D_{11}} \right\rfloor \tag{7}$$

$$u_2 = \left\lfloor D_{21} * \left\lfloor \frac{-q_1}{D_{11}} \right\rfloor + q_2 \right\rfloor \qquad j_2 = \left\lfloor \frac{-D_{21}}{D_{22}} * \left\lfloor \frac{-q_1}{D_{11}} \right\rfloor - \frac{q_2}{D_{22}} \right\rfloor$$

In general, an n-dimensional (n-D) case can be found in the same way by breaking the problem down into smaller matrices. The n-D case leads to n levels of the modulus transform. Clearly this procedure takes an exponential amount of computation and space.

In [8] a new graph-based method was introduced called the complementarity decision diagram (CDD) to reduce the computation and space by sharing these n levels of sub-expressions. For relatively large circuits, this technique can be orders of magnitude more efficient than the original method.

3. MNA FORMULATION OF PWL CIRCUITS AS THE MIXED LINEAR COMPLEMENTARITY PROBLEM

To facilitate the MNA formulation, we can represent the device described by the equations in (2) as a network of linear resistors, ideal voltage sources, and orthoators as shown in Figure 3.

The first piece with slope m_0 in Figure 2, is represented in Figure 3 by a resistor of value $1/m_0$ and a voltage source whose value is in terms of the slope and the extrapolation of that piece to the current axis ($f(0)$). This is the starting piece for PWL modeling. Each branch in this circuit represents a slope update on the previous piece in the PWL curve, which means that a new piece is reached once a new branch is turned on. Using this technique, any PWL circuit can be represented by a circuit consisting of a set of linear elements, (controlled) sources and orthoators.

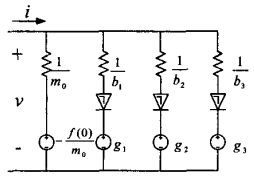


Figure 3. Network representing the PWL curve in Figure 2.

The MNA method then can be applied to solve PWL problems with an appropriate stamping rule for the orthoators. During the MNA stamping, orthoators are treated as special voltage sources. The voltage across an orthoator is u while its current is j. So, in MNA stamping, u goes to the right-hand side (RHS) of the MNA formulation while j is treated as an extra current variable. Noting that an orthoator is generally connected in series with a linear resistor and a voltage source (directly coming from the PWL mapping for circuit representation to realize the slope update), we can further treat them together as a macro circuit element. The compact MNA stamping for such a macro circuit element is as in Figure 4:

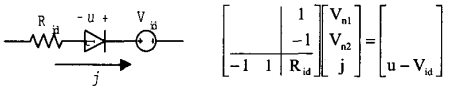


Figure 4. MNA stamping rule for the orthoator.

In general, the MNA formulation of PWL circuit equations can be written in the following *mixed linear complementarity problem* (MLCP) matrix:

$$\begin{bmatrix} \mathbf{M} & \mathbf{A} \\ -\mathbf{A}^T & \mathbf{N} \end{bmatrix} \begin{bmatrix} \mathbf{x} \\ \mathbf{j} \end{bmatrix} = \begin{bmatrix} \mathbf{b} \\ \mathbf{u}-\mathbf{o} \end{bmatrix}$$

$$\mathbf{j}^T\mathbf{u} = 0 \text{ and } \mathbf{j}, \mathbf{u} >= 0 \qquad (8)$$

where $\mathbf{x}$ is the vector of MNA nodal voltages and extra current variables, $\mathbf{j}$ is the vector of current variables of orthoators, $\mathbf{b}$ is the RHS vector of voltage sources and current sources, $\mathbf{u}$ is the vector of voltages across orthoators, $\mathbf{o}$ is the vector of voltages across voltage sources related to orthoators. The matrix $\mathbf{M}$ is the equivalent admittance matrix with all orthoators open or off. $\mathbf{A}$ is the incidence matrix of orthoators. $\mathbf{N}$ is the resistance matrix of linear resistors related to orthoators.

Suppose there are m orthoators and n MNA variables. Then the matrix $\mathbf{M}$ is of rank $n*n$, matrix $\mathbf{A}$ is of rank $m*n$, matrix $\mathbf{N}$ is of rank $m*m$. It should be noted here that matrix $\mathbf{A}$ is a very sparse matrix with at most two non-zero elements in each column, and matrix $\mathbf{N}$ is just a diagonal. If $\mathbf{M}$ is not singular, we can eliminate $\mathbf{x}$ from (8). This allows the MLCP matrix to be converted to a standard LCP as considered by van Bokhoven and Leenarets in [7]:

$$\mathbf{u} = \mathbf{D}\mathbf{j} + \mathbf{q} \qquad (9)$$

where $\mathbf{D} = \mathbf{A}^T\mathbf{M}^{-1}\mathbf{A} + \mathbf{N}$, $\mathbf{q} = -\mathbf{A}^T\mathbf{M}^{-1}\mathbf{b} + \mathbf{o}$. Noting that $\mathbf{M}$ and $\mathbf{A}$ are both sparse admittance matrices, the matrix $\mathbf{D}$ and the vector $\mathbf{q}$ can be computed from at most four cofactors of the matrix $\mathbf{M}$ and its determinant. Since typical analog circuits only require a few orthoator macro circuits to represent the nonlinearity, then, only some cofactors and the determinant of matrix $\mathbf{M}$ need to be represented symbolically. This can be implemented efficiently using determinant decision diagrams introduced originally by Shi and Tan in [11].

4. EXPERIMENTAL RESULTS

The proposed new method has been implemented into a prototype CAD program. Results from applying the resulting program to a behavioral model of the μa741 and a generic hard nonlinearity is presented in this section. For all the examples, our program reads in the circuit description in the SPICE-like format, sets up the MLCP formulation based on the framework of MNA, and then constructs symbolically all the solutions. Numerical results are obtained by repetitively evaluating the resulting symbolic expressions. We use the numerical simulations as a form to validate the symbolic expressions.

a) Example 1

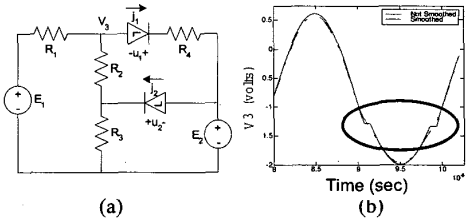
The first example is a generic circuit that behaviorally models a strong nonlinearity. In other words, our output waveform should exhibit abrupt changes in its behavior. To compare this to SPICE-like algorithms we also implemented a smoothing algorithm, which is commonly performed for numerical simulators. The smoothing algorithm implemented was formulated in [6], which replaces the absolute operator by a hyperbolic cosine as done in [6]. Note that the modulus transform is related to Chua's model by

$$|w| = \frac{(u+j)}{2}, \quad w = \frac{(u-j)}{2} \rightarrow \lfloor x \rfloor = \frac{(|x|+x)}{2} \qquad (10)$$

So $\lfloor x \rfloor$ is replaced with the following:

$$\lfloor x \rfloor \rightarrow \frac{\left(\frac{1}{\kappa}\ln(\cosh(\kappa x)) + x\right)}{2}, \qquad (11)$$

where κ is the smoothing parameter. The closer κ is to zero the closer the expression evaluates to $\lfloor x \rfloor$. To illustrate the effect of the smoothing function the circuit in Figure 5a is simulated. Since there are two orthoators used in this example, then we are solving a 2-D LCP matrix as in (12). The symbolic expression representing the voltage at node V_3 is shown in equation (13), notice the expressions representing the voltage across the orthoators are encapsulated by the modulus transform.



(a) (b)

Figure 5. (a) Circuit used for smoothing analysis. (b) A section of the transient analysis.

$$\begin{bmatrix} u^1 \\ u^2 \end{bmatrix} = \begin{bmatrix} \frac{R_1R_2+R_1R_3+R_1R_4+R_2R_4+R_3R_4}{R_1+R_2+R_3} & \frac{-R_1R_3}{R_1+R_2+R_3} \\ \frac{-R_1R_3}{R_1+R_2+R_3} & \frac{R_1R_3+R_2R_3+R_1R_4}{R_1+R_2+R_3} \end{bmatrix} \begin{bmatrix} j^1 \\ j^2 \end{bmatrix} + \begin{bmatrix} \frac{-(R_2+R_3)}{R_1+R_2+R_3}E_1+E_2 \\ \frac{R_3}{R_1+R_2+R_3}E_1-E_2 \end{bmatrix} \qquad (12)$$

$$V_3 = \frac{\left(E_1R_2R_4+E_2R_4(R_1+R_2)-\left[\frac{-R_1R_3}{R_1+R_2+R_3} * \left[\frac{-R_3E_1+(R_1+R_2+R_3)E_2}{R_3R_1+R_3R_2}\right] - \frac{(R_2+R_3)}{R_1+R_2+R_3}E_1+E_2\right]R_1R_2\right.}{R_2R_4+R_1R_4+R_1R_2} \left. + \left[\frac{-R_1R_3}{R_1+R_2+R_3} * \left[\frac{(R_2+R_3)E_1-(R_1+R_2+R_3)E_2}{R_1R_2+R_1R_3+R_1R_4+R_2R_4+R_3R_4}\right] + \frac{R_3}{R_1+R_2+R_3}E_1-E_2\right]R_1R_4\right) \qquad (13)$$

A transient sweep is performed and the waveform at node V_3 is shown in Figure 5b. The solid curve is the results of using the

modulus transform, while the dotted curve is the results from using the smoothing function. The smoothing parameter, κ, was set to 1. The smoothing function smoothes out the glitches seen in the modulus transform data as shown in the solid circle in Figure 5b. Taking the Fast Fourier Transform (FFT) of this data reveals differences in the distortion components. The normalized harmonic (HD) and intermodulation (IM) distortion components are shown in Figure 6. *What is opposite to the intuition is that smoothing actually yields larger distortion of the magnitude at third order harmonics and intermodulation distortions.*

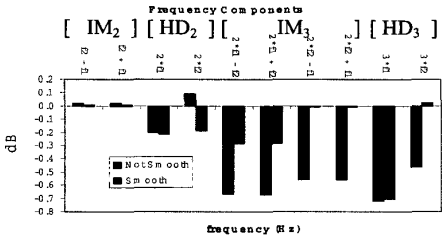


Figure 6. HD and IM distortion components of the Figure 5.

b) Example 2

The second example is a commonly used μa741 behavioral model shown in Figure 7 [13]. Note that it contains a nonlinear output resistor to simulate output limiting and a nonlinear transconductance simulating slew rate limiting. The parameters used for the model are taken from [13]. Figure 8a shows the time-domain waveforms when the input is a small-signal sin waveform computed by our method (PWL) and by SPICE. Clearly we can see that SPICE's smoothing leads to an over-estimation of the signal magnitude. Figure 8b shows the computed nonlinear behaviors when the input is applied to a large signal by both our method and SPICE. In this case, both simulators captured the limiting behaviors.

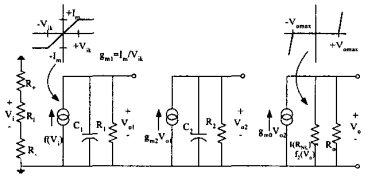


Figure 7. μa741 behavior model.

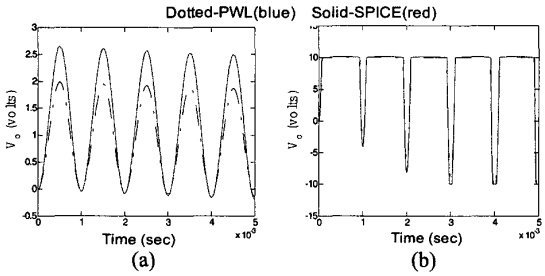


Figure 8. (a) μa741 result with the V_{in} amplitude = $1mV$. (b) μa741 result with the V_{in} amplitude = $0.1V$.

The harmonic distortion components of the μa741 time-domain results in Figure 8 are shown in Table 1. This clearly shows that SPICE and PWL obtain very similar results.

Table 1. Normalized Harmonic distortion of μa741.

Simulator	Fundamental	HD_2	HD_3
PWL	35.2808	0.9099	0.7274
Spice	35.2362	0.9102	0.7317

5. Conclusions and Future Work

In this paper, we presented a method for analyzing circuits with device and model hard nonlinearity characterized by piece-wise linear (PWL) I-V functions. The method is based on the modified nodal formulation of PWL circuits, where PWL devices are replaced by a network of linear resistors, (controlled) sources and orthoators. The resulting formulation is known as a mixed linear complementarity problem (MLCP), which can be converted to a standard LCP by implementing a determinant-decision diagram based procedure. Complementarity-decision diagrams were used to exploit the sharing of common sub-expressions of the LCP functions. The method has been implemented as a prototype tool and tested on a number of circuits.

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