A COUPLED ITERATIVE/DIRECT METHOD FOR EFFICIENT TIME-DOMAIN SIMULATION OF NONLINEAR CIRCUITS WITH POWER/GROUND NETWORKS^{*}

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Abstract: A coupled iterative/direct circuit analysis method is proposed for efficient SPICE-accurate time-domain simulation of nonlinear circuits with large-scale power/ground networks. The system under study is partitioned into a linear part including power/ground networks, a nonlinear part, and an interface between them. The part of power/ground networks is formulated by nodal analysis based on RCLK elements, and solved by an efficient conjugate gradient iterative method with an incomplete Cholesky decomposition preconditioner. The nonlinear circuit part is formulated by modified nodal analysis, and solved by the direct method as in SPICE. The iterative method and the direct method are coupled by a Gauss-Seidel like relaxation scheme with SPICE builtin varying time step-size numerical integration. How the condition number of a circuit matrix changes with time step-sizes is further studied. Experimental results on digital circuits with power/ground networks demonstrate that the proposed coupled iterative/direct method vields SPICE-like accuracy with orders of magnitude speedup for circuits with tens of thousands elements.

1. INTRODUCTION

With the increasing operation frequency, lower supply voltage and smaller device feature size, the effects of power/ground networks, such as *Ldi/dt* drop, *IR* drop, resonance, are becoming more and more pronounced [5]. An improper circuit design neglecting power/ground networks and packaging will result in excessive voltage drops and fluctuations in circuit supply nodes. The noise margin for digital circuits is therefore reduced, which may unfortunately disturb gate delays or even produce logic errors. The increasing demand to integrate digital, analog and radio frequency (RF) circuits into one single chip requires accurate analysis of VLSI circuits together with power/ground networks [1][3][5][9]. For such purposes as well as high fidelity coupled circuit and electromagnetic modeling [7], SPICE-like simulators are desirable for accurate transistor-level time-domain simulation.

However, efficient simulation of such systems presents a complexity challenge to SPICE [4]. To accomplish transient simulation, SPICE uses numerical integration formulae at each time point and applies the Newton-Raphson (NR) method to linearize nonlinear devices. Then the circuit system is simulated at each time point by solving a system of linear equations Ax = b, where A is typically in the form of a so-called modified nodal analysis (MNA) circuit matrix. It is well known that device evaluation dominates the simulation of small to medium scale circuits and can be speeded up using table-lookup nonlinear device models or parallel computation techniques. However, for large scale nonlinear circuits coupled with power/ground networks, the per-iteration cost of

transient simulation with SPICE is dominated by LU factorization of the circuit matrix A.



Figure 1. The circuit matrix structure of a power/ground example (a) before LU factorization and (b) after LU factorization.

Figure 1 (a) and Figure 1 (b) show the circuit matrix structure before and after LU factorization for a power/ground analysis example in Section 4. It can be seen that the original circuit matrix before factorization is very regular and sparse (9618 elements in a 1177x1177 matrix, which means the sparsity is 0.70%), while the matrix after factorization becomes irregular and much denser (89733 elements, the element number is increased 9.33X due to fillins and the sparsity becomes 6.68%). Therefore, a key idea to achieve speedup and save memory is to apply efficient krylov-subspace based iterative methods [1][5][9] on power/ground networks analysis since those methods only require matrix-vector multiplications on the original sparse circuit matrix.

Although iterative methods have been shown to be efficient for transient simulation of large-scale power/ground networks [1], their application to general nonlinear circuits is limited. The reason is that the circuit matrix for a nonlinear circuit is typically not symmetric positive definite, which prohibits the usage of efficient preconditioners for iterative methods. Iterative methods without good preconditioners are well known to have the convergence problem. The direct method based on the Newton-Raphson iteration as in SPICE is still the most efficient way for general nonlinear circuit simulation.

Noticing different application areas of iterative and direct methods, we present a new coupled iterative/direct method capable of analyzing nonlinear circuits with power/ground networks *in SPICE-like accuracy yet orders of magnitude speedup*. The system under study is partitioned into three parts – a linear part including power/ground networks, a nonlinear part and an interface between them. Two key ideas are:

- For power/ground networks, nodal analysis (NA) formulation of *RCLK* elements is applied so that an efficient iterative conjugate gradient method with an incomplete Cholesky decomposition preconditioner [1][6] can be used. For different circuit formulation methods, how the condition number of a circuit matrix changes with time step-sizes is further studied.
- 2) For nonlinear circuits, the modified nodal analysis (MNA) formulation is applied and the direct method as in SPICE is

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used. The iterative method and the direct method are coupled together by a Gauss-Seidel style relaxation scheme [8].

This paper is organized as follows. Section 2 proposes the new coupled iterative/direct method. The NA formulation for iterative methods and the condition number variation with time step-sizes are described in Section 3. Experimental results on digital circuits with power/ground networks are shown in Section 4. Section 5 concludes this paper.

2. THE COUPLED ITERATIVE/DIRECT METHOD

The system under study is shown in Fig. 2, in which power/ground networks are coupled with nonlinear circuits through a linear interface. It can be seen that parasitic coupling effects between the power network and the ground network are also incorporated. The linear interface is constructed so that only a few linear elements (such as resistors connecting grid nodes of power/ground networks and supply nodes of nonlinear circuits) are introduced.



Figure 2. Nonlinear circuits coupled with power/ground networks.

Figure 3 shows the related circuit matrix structure for the system in Fig. 2. Y_{PG} , Y_N and Y_I represent circuit matrices of power/ground networks, nonlinear circuits, and the interface, respectively. C_{PG} and C_{PG}^{T} are coupling matrices between power/ground networks and the interface. C_N and C_N^T are coupling matrices between nonlinear circuits and the interface. All other parts in the circuit matrix are zero. The unknown variables v and the right hand side (RHS) vectors **b** are also labeled accordingly.



Figure 3. The circuit matrix structure for a system in Fig. 2.

The circuit matrix Y_{I} for the interface can be further partitioned as below.

$$\boldsymbol{Y}_{I} = \begin{bmatrix} \boldsymbol{Y}_{INN} & \boldsymbol{Y}_{INP} \\ \boldsymbol{Y}_{IPN} & \boldsymbol{Y}_{IPP} \end{bmatrix}$$

where Y_{INN} and Y_{IPP} are self-admittance matrices for the ports of nonlinear circuits and those of power/ground networks, respectively, Y_{IPN} and Y_{INP} are coupling matrices between the ports of nonlinear circuits and those of power/ground networks. In general, Y_{IPN} = Y_{INP}^{T} .

To introduce the Gauss-Seidel style relaxation scheme [8], we regroup circuit sub-matrices and sub-vectors as below,

$$Y_{PG}^{*} = \begin{bmatrix} Y_{PG} & C_{PG} \\ C_{PG}^{T} & Y_{IPP} \end{bmatrix} Y_{N}^{*} = \begin{bmatrix} Y_{N} & C_{N} \\ C_{N}^{T} & Y_{INN} \end{bmatrix}$$
$$v_{PG}^{*} = \begin{bmatrix} v_{PG} \\ v_{Port-PG} \end{bmatrix} v_{N}^{*} = \begin{bmatrix} v_{N} \\ v_{Port-N} \end{bmatrix}$$
$$b_{PG}^{*} = \begin{bmatrix} b_{PG} \\ b_{Port-PG} \end{bmatrix} b_{N}^{*} = \begin{bmatrix} b_{N} \\ b_{Port-N} \end{bmatrix}$$

Therefore, the circuit matrix in Fig. 3 can be further written in the following format,

$$Y_{PG}^{*}v_{PG}^{*} = b_{PG}^{*} - Y_{IPN}v_{Port-N}$$
(1)
$$Y_{PG}^{*} + b_{PG}^{*} + b_{PO}^{*} + b_{PO}^{$$

 $\boldsymbol{Y}_{N}^{*}\boldsymbol{v}_{N}^{*} = \boldsymbol{b}_{N}^{*} - \boldsymbol{Y}_{INP}\boldsymbol{v}_{Port-PG}$ (2)

According to Eq. (1), once v_{Port-N} is fixed, v_{PG}^* can be solely solved. After v_{PG}^* (and therefore $v_{Port-PG}$) is given, v_N^* (and therefore v_{Port-N} can be determined by Eq. (2). Then, the new v_{Port-N} is compared to the old *v_{Port-N}* used during solving Eq. (1) to check if this Gauss-Seidel relaxation is converged. The coupled iterative/ direct method is summarized in Table I.

Table 1. The coupled iterative/direct method.						
INITIALIZATION:						
Construct Y_{INP} and Y_{IPN}						
<i>t</i> =0						
WHILE $(t < T_{\text{final}})$						
OUTER LOOP: do {						
Construct matrix Y_{PG}^* and vector b_{PG}^*						
Apply ICD-CG to compute v_{PG}^* based on v_{Port-N} using Eq. (1)						
INNER LOOP: do{						
Construct matrix Y_N^* and vector \boldsymbol{b}_N^*						
Apply NR linearization and solve Eq. (2)						
$\}$ while (v_N^* not converge)						
} while (<i>v_{Port-N}</i> not converge)						
Determine the next time step-size h_n						
$t = t + h_n$						
3						

It can be seen that the costly simulation of power/ground networks is in the outer loop, while the cheap simulation of nonlinear circuits is in the inner loop. The number of inner nonlinear iterations under the Gauss-Seidel relaxation scheme is generally higher than that with SPICE, since several outer iterations may be required to achieve the final convergence. Even so, a great simulation speedup is still achievable since the cost of each inner nonlinear iteration is much lower than that of one SPICE nonlinear iteration. The reason is that the size of nonlinear circuits is reduced greatly with power/ground networks decoupled in our scheme. Further, the simulation of nonlinear circuits can be speeded up using table-lookup nonlinear device models or parallel computation techniques.

3. ITERATIVE METHODS WITH NA FORMULATION

The MNA formulation for circuit elements is widely used in modern circuit simulators based on direct methods. However, as shown in the Section 1, the simulation of power/ground networks presents a challenge for direct methods. Therefore, the NA formulation of RCL elements has been applied for power/ground network simulation based on iterative methods [1]. The NA formulation of R and C is the same as their MNA formulation. The NA formulation of L with the trapezoid numerical integration formula is shown in Fig. 4. It can be seen that the equivalent conductance is $h_n/(2L)$ rather than $(2L)/h_n$ in the MNA formulation. The mutual inductance can be incorporated easily by so called Kelements [2]. It has been proved that the circuit matrix with *RCLK* elements based on the NA formulation is symmetric positive definite [1][2]. Therefore, we have implemented the conjugate gradient (CG) method with an incomplete Cholesky decomposition preconditioner [1][6] (named by ICD-CG).



Figure 4. NA formulation of a linear inductor.

The RCL circuit example in Fig. 5, the structure of which is typical in power/ground networks, is used to study how the condition number of a circuit matrix changes with time step-sizes. As shown in Fig. 6, the condition number for the MNA formulation is becoming worse as the time step-size decreases (h_n is less than 1). The reasons are: 1) The MNA formulation of voltage sources introduces zero diagonal elements; 2) The self-admittance matrix element at node 1 is only contributed by a fixed resistor. Therefore, a tighter tolerance is required when time step-size becomes smaller with iterative methods [5]. If the voltage source E and the serial resistor R_1 in Fig. 5 are replaced by an equivalent Norton current source and a parallel resistor, the condition number is kept relatively small with time step-sizes cahnged, as shown in Fig. 6. Unfortunately, it is not suitable for iterative methods since the MNA formulation of a linear inductor either introduces a negative diagonal element or causes the circuit matrix asymmetric.





As mentioned previously, the circuit matrix with the NA formulation is symmetric positive definite, which should be suitable for iterative methods. However, in Fig. 6 the condition number for the NA formulation is becoming worse with the time step-size increased (h_n is larger than 1). The reason is that the effects of linear inductors become ignorable with an enlarged time step-size – an enlarged equivalent conductance of $h_n/(2L)$ means a reduced equivalent resistance. In this case, linear inductors are close to short branches, which will cause excessive numerical errors with the NA formulation. Therefore, proper window-based truncation techniques on inductance matrices [2] should be applied before using the NA formulation so that ignorable (mutual) inductors are not present.

Once ignorable (mutual) inductances are truncated, it will be safe enough to use the NA formulation since the time step-size h_n is determined by time constants with relatively small values in a circuit. Figure 7 shows the histogram of SPICE time step-sizes for the *RCL* circuit in Fig. 5. It can be seen that most time step-sizes are less than 1 and some are even less than 0.1. Therefore, the condition number of the circuit matrix is required to be relatively small for h_n less than 1. According to Fig. 6, the NA formulation does ensure

the condition number of the circuit matrix relatively small when the time step-size is decreased for h_n less than 1.











Figure 8. The power/ground analysis example.

In Fig. 8. the power and ground supply networks are modeled as two *RCL* mesh layers (parasitic coupling capacitors are not shown in Fig. 8). Between these two layers is a 20-stage inverter chain, different inverters of which are connected to different power/ground grid nodes. Furthermore, *RCL* loads are added for each inverter to model interconnect lines between adjacent stages.

Figure 9 shows the transient output waveform of the inverter chain when the output signal is digital "1" (the high voltage level). The "1" signal has been disturbed due to the *IR*-drop (the input Vdd is 3.3v) and L*dI/dt effects of the power/ground network. Table II shows the simulation results with varied numbers of elements

modeling the power/ground network. In our experiments, the size of two RCL meshes is changed to vary the number of elements. The run time comparison between SPICE3 and the proposed method with the tolerance of the iterative method set to 1e-6 and 1e-8 is shown in Fig. 10. We can see that the coupled iterative/direct method achieves more speedup for larger circuits. The maximum overall speed-up reach 85.39X and 16.74X (with about 60 thousand elements) with the tolerance set to 1e-6 and 1e-8, respectively. The speedup is comparable to a recent explored direct method [3].



Figure 9. Transient output waveform of the inverter chain for power/ground analysis example.



It can be seen from Table II that the number of outer Gauss-Seidel iterations is typically increased to 4X to 5X of that of SPICE nonlinear iterations. When the tolerance is set to 1e-6, the average number of CG iterations for each Gauss-Seidel step is 6.5 to 9, and it becomes 22 to 45 if the tolerance is set to 1e-8. The number of CG iterations increases dramatically to achieve high accuracy, i.e., when the tolerance is set to 1e-8. One way to improve the

performance of iterative methods on large-scale power/ground networks for high accuracy is to apply multigrid-like methods [9].

5. CONCLUSION

A coupled iterative/direct time-domain circuit analysis method has been proposed for nonlinear circuits coupled with large-scale power/ground networks. Nodal analysis formulation of RCLK elements is applied on power/ground networks and an efficient iterative conjugate gradient method with an incomplete Cholesky decomposition preconditioner is used. Modified nodal analysis formulation is applied on nonlinear circuits and the direct method based on the Newton-Raphson iteration is used. The iterative method and the direct method are coupled together by a Gauss-Seidel style relaxation scheme. We further studied how the condition number of a circuit matrix changes with time step-sizes. Experimental results on digital circuits with power/ground networks show that the proposed method yields SPICE-like accuracy with orders of magnitude speedup over SPICE3.

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#Elems	SPICE3		Coupled Solver						Speedup	
			ε=1e-6			ε=1e-8			<u> </u>	<u> </u>
	#Iter	Overall (sec)	#GS Iter	#CG Iter	Overall (sec)	#GS Iter	#CG Iter	Overall (sec)	8– 1e-6	د_ 1e-8
4002	4016	456.51	17363	113832	79.30	17350	384444	242.43	5.76	1.88
8851	4171	1.75e3	16432	128561	183.34	16205	475429	647.25	9.55	2.70
34802	3986	6.17e4	17679	156038	869.80	17868	772263	3.88e3	70.94	15.90
61602	4377	1.52e5	20208	162416	1.78e3	22335	1002260	9.08e3	85.25	16.74

Table II. Simulation results for the power/ground analysis example.