

AN SCR-GTO MODEL DESIGNED FOR A BASIC LEVEL OF MODEL PERFORMANCE

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Abstract - The SCR-GTO model in this paper is specifically designed to meet the performance features proposed for the basic performance level. An innovative and unique *Quasi-Physical* modeling technique combines a behavioral switch model and a physical diode model to avoid the convergence difficulties which can occur when regenerative thyristor models are used. A standard benchmark circuit is proposed for validating the switching performance of SCR and GTO models.

I. INTRODUCTION

In this paper, an innovative and unique *Quasi-Physical* modeling technique is used to design an SCR-GTO model to meet a basic level of model performance. Unlike the commonly used behavioral and two-transistor thyristor models found in most SPICE-based simulators [1]-[5], this quasi-physical SCR-GTO model has all the features proposed for a basic model. A recently proposed procedure [6] for specifying model performance for different simulation applications describes the basic model as one which gives typical dynamic characteristics with only a few simple equations. Table I presents four of the proposed model validation levels for SCR and GTO devices from [6].

Most basic level SCR-GTO models use two BJT's or three diodes in a regenerative switch including additional resistors, capacitors, diodes, and controlled sources in a macromodel [1]-[5]. These models lack reverse recovery, and their negative resistance characteristic creates numerical convergence difficulties in many simulators because the switching transients cannot be easily controlled. Their unreasonably fast switching times tend to produce simulation artifacts or simulation failures. Also, their omission of reverse recovery invalidates the estimation of switching power losses and conducted EMI [7]. Model performance at the basic or level 1 level indicated in Table I is essential for

applications where approximate waveform accuracy is sufficient and fast simulation is still crucial.

The new SCR-GTO model presented here provides performance at this basic level and avoids the problems due to the negative resistance region of the older models. A combined charge based and behavioral modeling approach is used to obtain a relatively simple and compact model. The model is applied to the simulation of a Solid-State Breaker [8] which is one of the new Custom Power Devices under development with EPRI sponsorship.

TABLE I

Four of the Proposed Model Validation Levels for the SCR and GTO

Level	Features	Circuit Applications
0 Ideal Switch	Static, ideal switch	System dynamics where many switching cycles must be simulated, control circuit design.
1 Basic	Basic static & dynamic characteristics. - Reverse recovery, continuous current and voltage during commutation.	General use where approximate waveform accuracy is satisfactory. An advantage of these models is easy parameter extraction.
2 Accurate	Accurate dynamic characteristic within the device SOA - Static and transient negative resistance, reverse tail current, quenching time, conductivity modulation, dynamic turn-on, dynamic turn-off (GTO only)	Switching power dissipation Snubber design Stress EMI
3 Thermal	Dynamic thermal model - Dynamic temperature	Heat sink design, Thermal stress, thermal instabilities

II. THE QUASI-PHYSICAL MODELING TECHNIQUE

The quasi-physical SCR-GTO model consists of a **behavioral switch** model and a **charge-based diode** model (hence the name *quasi-physical*). Although it is an equation-based model, the approximate equivalent circuit shown in Fig. 1 diagrams its operation.

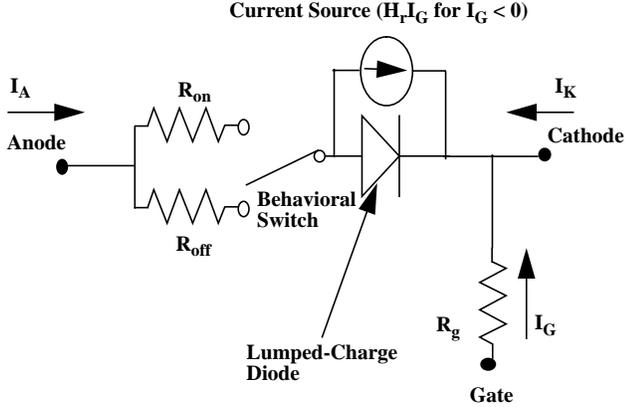


Fig. 1 Equivalent circuit representation of the Quasi Physical SCR-GTO model.

The same quasi-physical model can be configured to function either as an SCR or a GTO through the turn-off gain parameter H_r , which determines whether the model functions as an SCR or a GTO. For an SCR model, the parameter H_r is set to zero. The current source arrow in Fig. 1 depicts the current flow direction during application of a negative gate current during turn-off of a GTO. The resistor R_g , represents the gate impedance of the device. The complete SCR-GTO model contains only five analog equations ((3) - (7)). These equations have been carefully chosen to obtain moderate accuracy, easy parameter extraction and minimum simulation time. The following sections discuss the modeling approach and model equations.

A. Behavioral Switch

The negative resistance region in a thyristor's i - v characteristic often causes numerical instability and convergence difficulties in simulation. By using an exponentially changing impedance as shown in Fig. 2 the troublesome negative resistance effects can be avoided. The gradual change of an exponential transition models the turn-on transient of the thyristors better than the almost instantaneous change from a negative resistance model. This approach provides excellent numerical stability and model robustness.

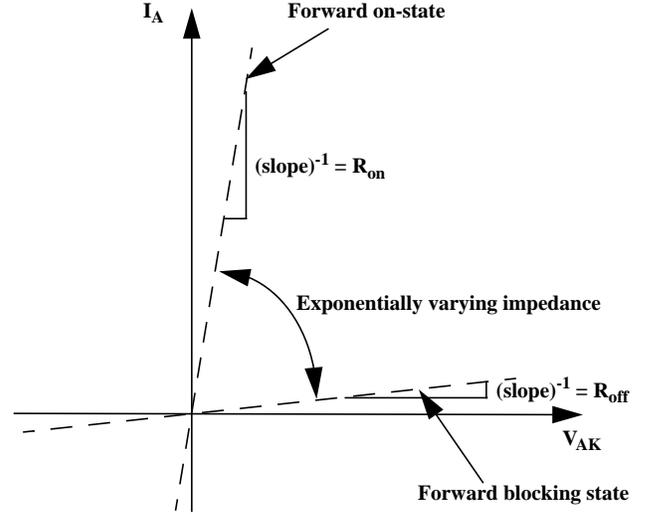


Fig. 2 Switching between conducting and non-conducting states by means of an exponentially changing impedance.

The exponential transition in the impedance has the form given by (1) and (2). Note that (2) assumes that $R_{on} \ll R_{off}$. The parameters, Res_{on} and Res_{off} , denote the static on- and off-state resistances of the thyristor, respectively.

$$Res_{on} = (R_{off} - R_{on}) \cdot \exp\left(-\frac{(t - tb_1)}{\tau_1}\right) + R_{on} \quad (1)$$

$$Res_{off} = ((1-x) \cdot R_{on}) + \frac{1}{\alpha \cdot \exp\left(-\frac{(t - tb_2)}{\tau_2}\right) + \beta} \quad (2)$$

where,

$$\beta = \frac{1}{R_{off} - ((1-x) \cdot R_{on})}$$

$$\alpha = \frac{1}{x \cdot R_{on}} - \frac{1}{R_{off}}$$

The quantities, tb_1 and tb_2 , represent the time instants at which the transitions from off-to-on-state and on-to-off-state occur, respectively, while R_{on} and R_{off} denote the default values assigned to the static on- and off-state impedances, respectively. The parameters, τ_1 and τ_2 , denote the rate of change in the impedances and affect the turn-on and turn-off time. The factor x where $0.4 < x < 0.6$, is used to slow the initial rate of rise from R_{on} . A suggested value for x is 0.5. As mentioned, the exponential functions in (1) and (2) are carefully chosen to provide optimum numerical stability by incorporating a gradual change at low impedance points such

as point A, and B as shown in Fig. 3. Since the numerical changes in the effective resistance values that occur during a switching transition are large, the gradual change in ‘Res’ avoids abrupt numerical changes for the simulator.

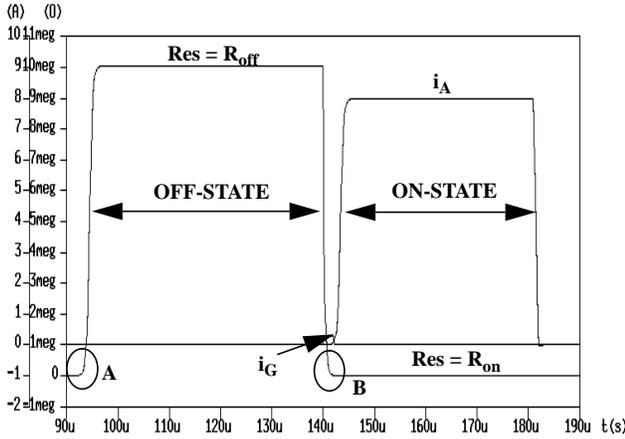


Fig. 3 The gradual change at low impedance points (pt. A and B) provides numerical stability.

B. Lumped-charge Diode

Unlike most physics-based models that utilize a large number of internal device geometry and doping parameters, the lumped charge modeling technique reduces the complexity while retaining the internal carrier transport processes and basic structural information of the device [9]. The lumped charge approach discretizes a device structure into several critical regions. ‘‘Charge’’ nodes and ‘‘junction’’ nodes are inserted into these regions accordingly. Charge nodes serve to model recombination and charge storage in the device whereas junction nodes relate charge values to junction voltage through the Boltzmann relations. A thorough explanation of the Lumped-Charge approach is documented in [9].

When a thyristor is conducting, its operation is similar to a p-i-n diode. The concentration of electrons and holes injected from the n^+ and p^+ regions are orders of magnitude larger than the contributions from the lightly doped n^- -drift and p^- -base regions (base of pnp and npn transistors) of the thyristor. Thus, the background doping in the base regions becomes insignificant and the internal charge distributions are similar to those in a p-i-n diode when conducting. Given this similarity of operation, the quasi-physical SCR-GTO model uses the previously developed Lumped-charge p-i-n diode model equations to model the thyristor’s on-state characteristics and reverse turn-off transients. The derivation of these equations is in [7] and [10]. Fig. 4 shows the doping profile during on-state along with the locations of charge nodes in the thyristor.

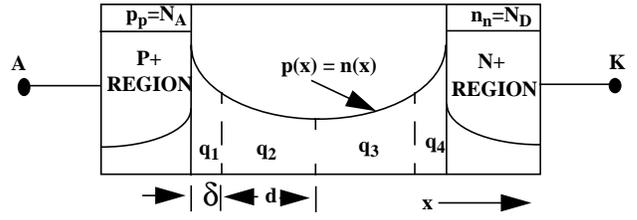


Fig. 4 Injected charge concentration and location of charge nodes in a thyristor during conduction. (after p-i-n diode in reference [10])

The important transient behavior of a thyristor that prompted the use of the Lumped-charge diode model is reverse recovery which occurs when a forward-biased thyristor is turned off rapidly. During this reverse recovery transient, charge q_1 and q_4 are exhausted first. Then, the internal stored charges such as q_2 and q_3 cause transient reverse current to flow at high reverse voltage. Reverse recovery is represented by (3)-(5). Equations (6) and (7) are derived from Kirchhoff Voltage Law (KVL) and Kirchhoff’s Current Law (KCL) to link internal variables to the terminals of the model. The parameters q_M and q_E denote the charge in the gate region and junction charge variable, respectively, and are given by $q_M = 2q_2$, and $q_E = 2q_0$, where q_0 represents the injected charge level at the p^+i junction. The parameter q_{M0} is equivalent to $I_s \cdot \tau_d$ while ϕ_t represents thermal voltage.

$$q_M = q_E - (i_a \cdot T_M) \quad (3)$$

$$0 = \frac{dq_M}{dt} + \frac{q_M - q_{M0}}{\tau_d} - i_a \quad (4)$$

$$q_E = q_{M0} \cdot \exp\left(\left(\frac{v_d}{n_o \cdot \phi_t}\right) - 1\right) \quad (5)$$

$$v_d = v_{ak} - (i_a \cdot Res) \quad (6)$$

$$i_k = -(i_a + i_g) \quad (7)$$

III. PARAMETER EXTRACTION

Most thyristor models fail to provide a systematic approach for extracting model parameters. The subcircuit models that are based on the regenerative connection of two-transistor approach [1]-[5] consist of many bipolar transistor parameters that have little correlation to the physical parameters of a thyristor. For these models, the user must thoroughly understand model development to extract the

model parameters. In contrast, parameter extraction of the quasi-physical SCR-GTO model is simple and straightforward.

The parameters of the quasi-physical SCR-GTO model are listed in Table II. The parameters V_{RM} , I_{GT} , I_H , and H_r can be obtained directly from a device data sheet. The parameter 'init_cond' allows users to set the initial condition of the device to either the on- or off-state. Two other important parameters are the switching time constants τ_1 and τ_2 which determine the rate of transitions between on- and off-states. Both these parameters are empirically fit to the switching transients. Typical values for both τ_1 and τ_2 are approximately 0.1 μ s.

TABLE II
Definition of Model Parameters

Parameter	Definition	Equation for parameter
V_{RM}	Breakover voltage	Data sheet
I_{GT}	Positive gate trigger current	Data sheet
I_H	Holding current	Data sheet
R_{on}	On-state impedance	(8)
R_{off}	Off-state impedance	(8)
Init_cond	Initial condition for setting initial state to either ON or OFF	User defined
τ_1	Switching time constant for on-state	User defined
τ_2	Switching time constant for off-state	User defined
H_r	Turn-off gain	Data sheet
τ_d	Carrier lifetime	ref. [10]
T_M	Transit time	ref. [10]
I_S	Diffusion leakage current	ref. [10]
n_o	Emission coefficient	ref. [10]

Of the thirteen user-defined parameters, only six (R_{on} , R_{off} , τ_d , T_M , I_S , n_o) are extracted from experimental data. Equation (8) is used to determine parameters R_{on} and R_{off} . The anode-cathode voltage V_{AK} , and anode current I_A , can be obtained from a curve tracer i-v characteristic. Here, R_{on} and R_{off} are the slopes of the forward on-state and forward blocking state i-v curves, respectively, as shown in Fig. 2.

$$R_{on} \text{ or } R_{off} = \frac{V_{AK}}{I_A} \quad (8)$$

Carrier lifetime τ_d , and transit time T_M , can be extracted from SCR turn-off current waveforms like the typical inductive load turn-off waveform in Fig. 5. The approach for extracting these parameters is described in [10].

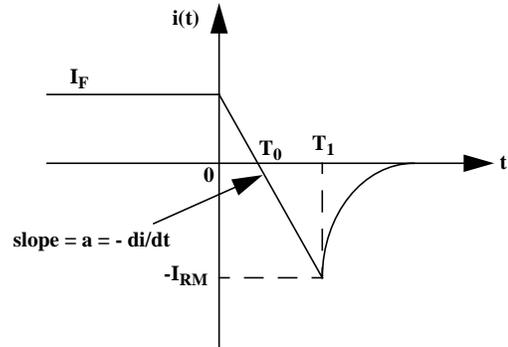


Fig. 5 Typical SCR turn-off current waveform. (after [9])

IV. SIMULATION RESULTS

A good benchmark circuit operates the model under maximum stress to test robustness and stability. The single phase controlled rectifier in Fig. 6 is proposed as a standard benchmark circuit for validating SCR models [[6], [11], [12]]. The dual circuit, an H-bridge in Fig. 10 is proposed as the benchmark circuit for validating GTO models [6].

A. SCR Test: A Single Phase Controlled Rectifier Circuit

A single phase bridge is preferred over a three phase bridge because the single phase circuit switches all legs of the bridge simultaneously which stresses the model more severely. The SCRs in the single phase controlled rectifier circuit undergo maximum stress during commutation when abrupt changes in voltage and current occur. Many thyristor models fail under such stress or produce unrealistic simulation artifacts. The simulation results in Fig. 7 and Fig. 8 show the robustness of the quasi-physical SCR model. Here, a continuous current and voltage can be seen while the four SCRs simultaneously commute. The inductive voltage spikes from reverse recovery of the SCRs are also visible. An SCR with a shorter carrier lifetime τ_d , or longer transit time T_M will exhibit smaller voltage spikes. A typical commercial two-transistor SCR macro-model is also tested in the circuit. The simulated result in Fig. 9 shows incorrect and excessive

voltage spikes during the switching of the SCRs. The oscillations observed at the spikes prolong simulation time and can cause convergence difficulties.

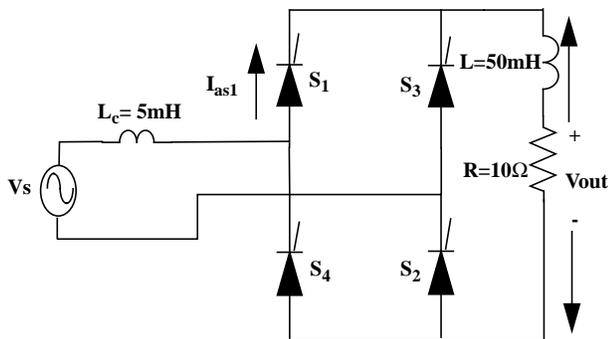


Fig. 6 A single phase controlled rectifier which is proposed as a benchmark circuit for testing SCR models.

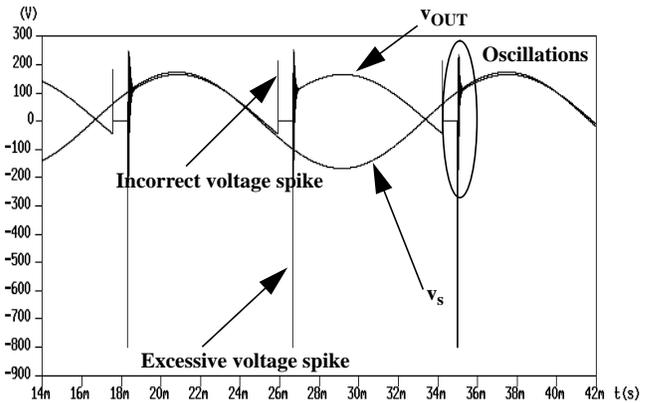


Fig. 9 Simulated output voltage using a commercial two-transistor SCR macro-model. Note the incorrect and excessive voltage spikes.

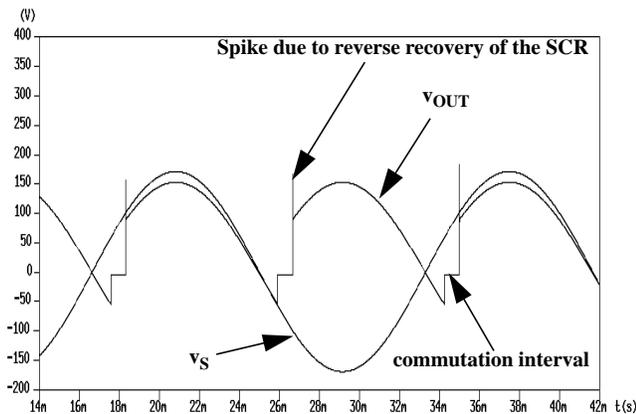


Fig. 7 Simulated output voltage V_{out} of the controlled rectifier circuit. Model parameters are: $\tau_1 = .1\mu s$, $\tau_2 = .1\mu s$, $\tau_d = 2.3\mu s$, $T_M = .15\mu s$.

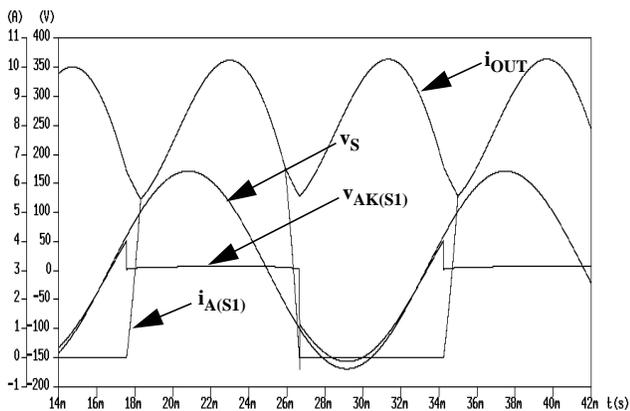


Fig. 8 Waveforms showing anode current $i_A(t)$, voltage across SCR S_1 $v_{AK}(t)$, and output current.

B. GTO Test: The H-bridge inverter circuit

The H-bridge inverter circuit in Fig. 10 is proposed as the benchmark circuit for testing GTO models. During the interval when G_1 and G_2 conduct, G_3 and G_4 endure high forward or reverse voltages across their anode-cathode terminals. The hard-switching that occurs when G_1 and G_2 turn-off produces a large power loss forcing the devices to undergo considerable stress. This circuit provides an excellent test for model robustness and stability. Note that reverse conducting diodes are included to provide a continuous conduction path (freewheeling). Simulation results are shown in Fig. 11 and Fig. 12.

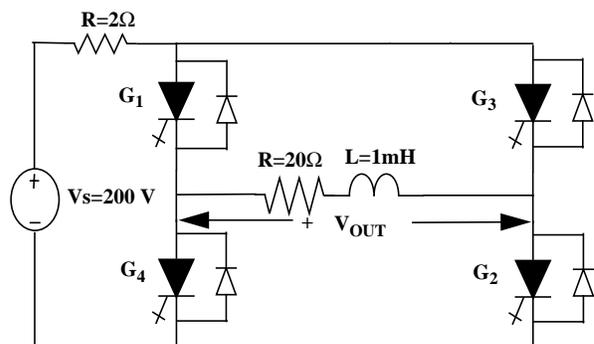


Fig. 10 An H-bridge inverter circuit proposed as benchmark circuit for testing GTO models.

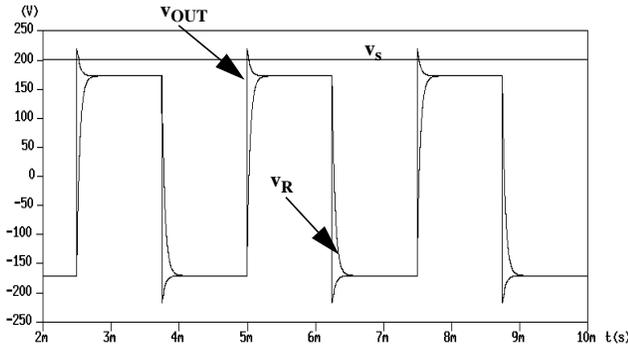


Fig. 11 Simulated output voltage v_{OUT} and voltage across the load resistor, v_R .

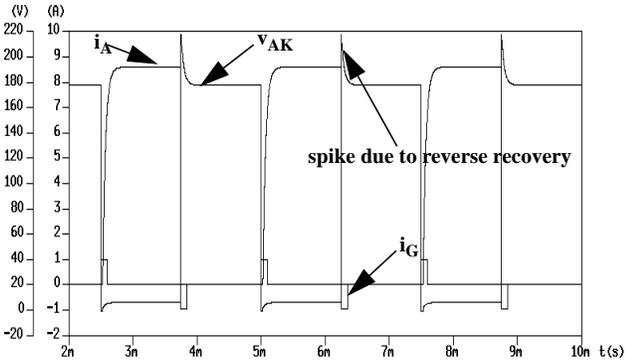


Fig. 12 GTO gate current i_G , anode current i_A , and anode-cathode voltage v_{AK} .

V. THE SOLID-STATE BREAKER

This section demonstrates a realistic application of the quasi-physical SCR-GTO model in the simulation of a Solid-State Breaker (SSB). The SSB is a Custom Power Device that utilizes fast switching power semiconductor devices to provide rapid response (within a small fraction of a cycle) to distribution system faults [8]. In the event of a fault, an SSB senses, opens and then automatically recloses its distribution circuit.

The SSB consists of pairs of GTOs and SCRs connected in antiparallel (Fig. 13). The GTO provides rapid interruption of a fault to protect a distribution circuit from destructive thermal and mechanical stresses caused by high fault currents. During the event of a fault, the GTO quickly interrupts the current. Simultaneously, the SCR turns on to provide a controlled path for the fault current. The SCRs are used to conduct the fault current for a limited number of cycles known as either the ‘fast’ or ‘slow’ operations; depending on the number of conduction cycles to attempt to clear the fault. The SCRs are then turned off, disabling the

SSB for an interval known as the ‘reclosing interval’ while the SCRs and distribution circuit are allowed to cool. If the fault still exists after a number of ‘slow’ or ‘fast’ operations, the SSB is disabled permanently to protect the distribution facility from further fault currents. If the fault clears during one of the conduction intervals of the SCRs, then the SCRs continue normal conduction until the slow or fast operation is completed. The GTOs then resume conduction.

Performance of the SSB is limited by the capabilities of its power semiconductor devices. During the interruption of a fault, the dynamics of the switching devices have a major effect on the circuit. Reverse recovery is essential to include in an SSB simulation because of its contribution to switching transients and internal SSB power dissipation. Speed in simulation is also crucial since many cycles must be simulated. The quasi-physical SCR-GTO model is designed for applications such as these.

The circuit shown in Fig. 13 below represents a simple single phase distribution system where the SSB is used as a protection device. The switch shown in the figure is used to create a line-to-ground fault in the distribution system. When the switch is closed the current flowing through the SSB will increase dramatically simulating a faulty condition. This switch is also used to control the time duration of the fault. The operation of the SSB is demonstrated in the simulation results shown in Fig. 14 - 16 for a permanent fault case. The spikes shown by ‘A’ in Fig. 14 and Fig. 15 represent GTOs turning on and off. Since the fault still exists, the GTOs immediately switch off after turn on to prevent destruction. Fig. 15 and Fig. 16 show the currents through the GTOs and SCRs, respectively. These figures show the GTOs interrupting the current during a fault and the SCRs providing a controlled path for the fault current.

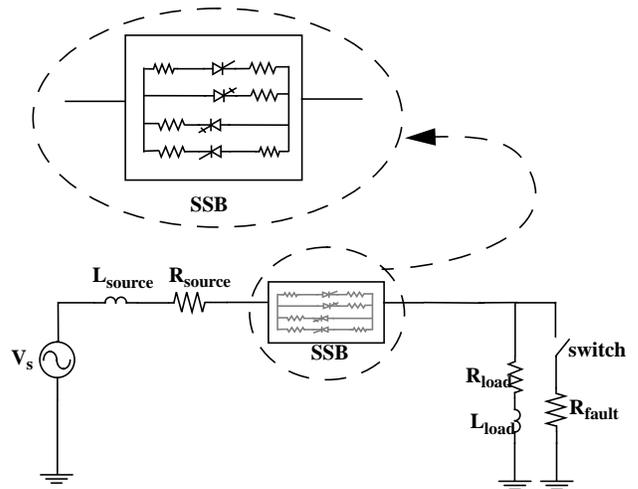


Fig. 13 Single phase distribution system with SSB.

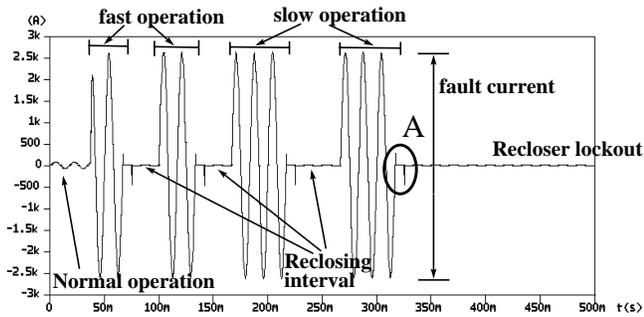


Fig. 14 Current flowing through the SSB for two slow and two fast operations. The spikes represent repeated attempts of the GTOs to turn on.

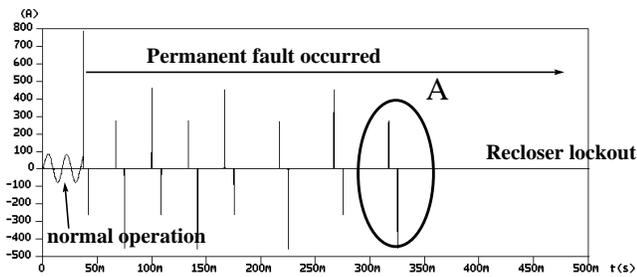


Fig. 15 Current flowing through the GTO devices in the SSB. During a fault, the GTOs turn off, limiting the fault current through them. The spikes represent repeated attempts of the GTOs to turn on.

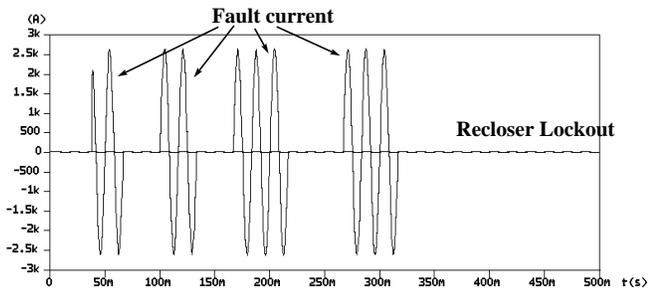


Fig. 16 Current through the SCRs in the SSB. During a fault the SCRs provide a conduction path to maintain fault current coordination in the distribution system.

VI. DISCUSSION

The SCR-GTO model is designed to turn on when the gate pulse i_G exceeds the default gate threshold current I_{GT} , a parameter obtainable from device data sheets. Similarly, the GTO is turned off when the gate current goes below the reverse gate trigger current I_{GREV} . In contrast, the SCR turn-off transients are modeled by the charge-based equations. The SCR is turned off when q_M goes below the holding charge $q_{hold} = I_H \cdot \tau_d$, a parameter derived from the holding current I_H .

The anode current of a thyristor does not respond

immediately after application of gate current. The turn-on time t_{on} , is shown in the simulated turn-on waveform characteristics of the quasi-physical SCR-GTO model (Fig. 17).

Compared to more advanced and complex SCR and GTO models, a limitation of the quasi-physical model is that the negative resistance region in the I-V characteristic is omitted. The model also lacks correlation between the gate current and the charge equations (see equations (3)-(5)). No restriction exists for minimum gate pulse width to turn-on the device as required in real devices. The derivation of the reverse recovery equations assumes that the device reverse recovery is independent of the reverse bias voltage. Some of the characteristics of the thyristor are neglected in the model to retain its simplicity. Among them are the omission of turn-on conductivity modulation. The voltage drop, V_{ak} , across the thyristor is also assumed to be independent of the amplitude of the gate current pulse. This model was developed for use in applications where reasonable accuracy is sufficient and fast simulation speed is important. More complex models exist when high accuracy is essential [13],[14].

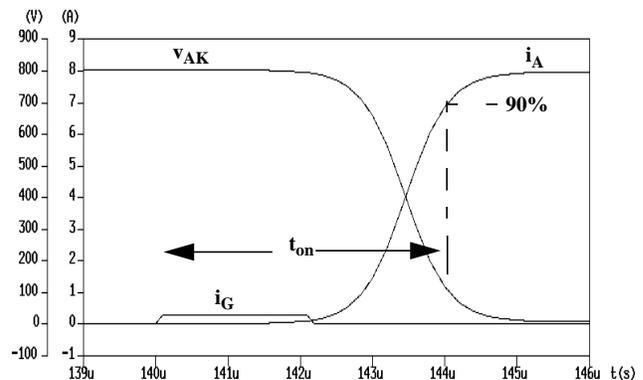


Fig. 17 The turn-on waveform of the quasi-physical SCR-GTO model. The time t_{on} is proportional to the rate of change in impedance (τ_1 and τ_2), carrier lifetime (τ_d), and transit time (T_M).

VII. CONCLUSION

A new class of simplified, reliable, and user-friendly models is now available to replace the existing basic two transistor models. Other high level (i.e. level 2 and higher) models such as detailed charge-based models are more accurate but simulate too slowly in complex circuits with many devices. The SCR-GTO model presented in this paper is specifically designed to meet the performance features proposed for the basic performance level [6]. The quasi-physical modeling approach is a unique technique which incorporates only essential device physics for simulating non-quasi-static effects, plus an exponentially changing resistance to avoid the simulation problems arising from

negative resistance effects which can occur in other models. All critical device behavior such as reverse recovery, and holding current are included. The quasi-physical modeling approach is also sufficiently simple to provide superior simulation speed and easy parameter extraction when compared to other models.

The robustness and stability of the SCR-GTO model are verified in two proposed benchmark circuits. A standard commercial two-transistor SCR macro-model was shown to perform poorly in the same benchmark circuit with excessive voltage spikes and simulation artifacts. The ‘standard’ two-transistor SCR model is no longer recommended for use in any application. One should either use an ideal switch model or a basic level SCR-GTO like the one introduced here.

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APPENDIX

A. Complete set of equations for the Quasi-physical SCR-GTO model

1) General equations:

$$v_{ak} = v(a) - v(k) \quad (A.1)$$

$$v_{gk} = v(g) - v(k) \quad (A.2)$$

$$i_g = v_{gk}/R_g \quad (A.3)$$

$$i_{grev} = -i_a/(10 \cdot H_T) \quad (A.4)$$

$$q_{hold} = i_{hold} \cdot \tau_d \quad (A.5)$$

$$q_{Mo} = I_s \cdot \tau_d \quad (A.6)$$

2) Off-to-On state (If $I_G > I_{GT}$ or $V_{AK} > V_{RM}$)

$$Res_{on} = \left(R_{off} - R_{on} \right) \cdot \exp\left(-\frac{(t - tb_1)}{\tau_1} \right) + R_{on} \quad (A.7)$$

3) On-to-Off state (If $q_M < q_H$ or $I_G > I_{GREV}$)

$$Res_{off} = \left((1-x) \cdot R_{on} \right) + \frac{1}{\alpha \cdot \exp\left(-\frac{(t - tb_2)}{\tau_2} \right) + \beta} \quad (A.8)$$

where,

$$\beta = \frac{1}{R_{off} - \left((1-x) \cdot R_{on} \right)}$$

$$\alpha = \frac{1}{x \cdot R_{on} - \frac{1}{R_{off}}}$$

4) On state (Lumped-charge diode equations)

$$q_M = q_E - \left(i_a \cdot T_M \right) \quad (A.9)$$

$$0 = \frac{dq_M}{dt} + \frac{q_M - q_{Mo}}{\tau_d} - i_a \quad (A.10)$$

$$q_E = q_{Mo} \cdot \exp\left(\left(v_d / \left(n_o \cdot \varnothing_t \right) \right) - 1 \right) \quad (A.11)$$

$$v_d = v_{ak} - \left(i_a \cdot Res \right) \quad (A.12)$$

$$i_k = -\left(i_a + i_g \right) \quad (A.13)$$