Modeling of Power Diodes with the Lumped-Charge Modeling Technique

Cliff L. Ma, *Member, IEEE*, Peter O. Lauritzen, *Senior Member, IEEE*, and Jakob Sigg

***Abstract*— The lumped-charge modeling technique is used to build a simple, physics-based power diode model for circuit simulators. The model consists of simplified, but fundamental semiconductor device equations. The important characteristics of power diodes under static and dynamic conditions are obtained in this compact and efficient model.**

***Index Terms*— Compact model, lumped-charge, power diode.**

I. Introduction

COMPARED to microelectronic devices, power semiconductor devices include wide, lightly doped regions for high-voltage operation. Several power diode models [1]–[6] have been developed in recent years to replace the standard SPICE diode model for accurate simulation of high-level injection and nonquasi-static effects, which are of particular importance in power electronic applications.

To include these features, two main approaches have been employed, physics-based analytical modeling [1]–[4] and hybrid modeling [5], [6]. The hybrid modeling approach solves the ambipolar diffusion equation in the lightly doped regions using numerical algorithms to evaluate carrier distribution under high-level injection conditions. Analytical equations are used for the rest of the regions. The spacial charge carrier distribution can be calculated with relatively high accuracy. However, computational cost is relatively high, device geometrical information is needed, low-level injection effects that are important during device turn-off are omitted, and parameter extraction is difficult. Alternatively, with the analytical modeling approach, the models are derived from simplified device physics. The resulting model equations are in relatively simple forms, which are easier to implement into circuit simulators and enable high computational efficiency. The model parameters can also be extracted from electrical measurements. But, the accuracy and performance of analytical models depend on how the fundamental equations are simplified.

The lumped-charge modeling technique [7], [8] represents a systematic technique for analytical modeling. The diode [1], [3], silicon-controlled rectifier (SCR) [9], gate turn-off (GTO) [10], MOS-controlled thyristor (MCT) [11], and MOSFET [12], [13] models have been created. This modeling technique leads to a significant reduction of model complexity while retaining the basic structural information and internal carrier transport processes in the device. The resulting models contain sets of continuous equations, which describe both static and dynamic operation.

This paper presents the basic lumped-charge modeling technique for power bipolar devices and constructs a power diode model using the technique. The goal is to establish a thorough understanding of this modeling approach and at the same time make it easy to use for model development. This diode model consists of simplified fundamental device equations in the lumped-charge form. It differs from [1] and [3] in terms of systematic construction and functional completeness. Sample simulation and experimental data are included. A parameter extraction technique is also provided.

Manuscript recieved January 8, 1996; revised October 14, 1996.

C. L. Ma is with Analogy, Inc., Beaverton, OR 97008 USA.

P. O. Lauritzen is with the University of Washington, Department of Electrical Engineering, Seattle, WA 98195-2500 USA.

J. Sigg is with Siemens AG, Corporate Research and Development, D-81739 Munich, Germany.

Publisher Item Identifier S 0885-8993(97)03294-8.

II. The Lumped-Charge Modeling Technique

External electrical characteristics of semiconductor devices are directly linked to internal carrier distributions and their transport characteristics. The lumped-charge modeling technique uses the following guidelines to simplify the fundamental semiconductor equations, which govern electron and hole behavior.

1) The device structure is discretized into several P- or N-type regions, each of which contains charge-storage and connection nodes. A charge-storage node is responsible for charge-carrier storage and recombination and is usually located near the center of a region; a connection node links junction voltage to the charge-carrier concentration level and is located on the junction-depletion edge.
2) The hole and electron charge values at each node are obtained by multiplying the local charge-carrier concentrations by the volume of the reference region, which is typically one of the lightly doped regions.
3) Finally, the charge nodes are linked using the following six equations from device physics and circuit theory:
   a) current density equations;
   b) current continuity equations;
   c) charge neutrality equations;
   d) Boltzmann relations (p-n junction equations);
   e) Poisson equations;
   f) Kirchoff current and voltage laws.

The first five describe carrier distribution and transport between the charge nodes in the device; the last connects internal variables of the model equations to terminal characteristics.

0885–8993/97$10.00 © 1997 IEEE

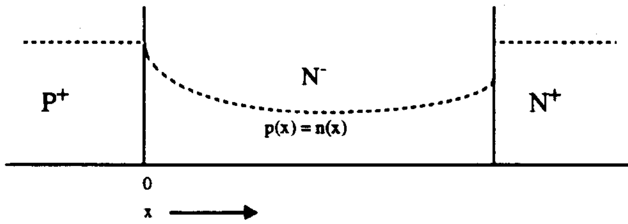


Fig. 1. 1-D injected charge distribution in a $P^+N^-N^+$ diode structure under high-level injection. Electron and hole carrier concentrations are identical $p(x) = n(x)$ in the N^- base region.

The fundamental model variables are charges and voltages. The current variables are derived from the charges and voltages using the above fundamental equations.

To keep the model simple, a small number of charge nodes should be chosen to represent the charge carrier distribution across the device. Typically, a minimum of one charge-storage node and two connection nodes is needed in each lightly doped region, where injected charge carrier distribution and variation determine the device static and dynamic characteristics. In heavily doped regions, only one charge node is necessary to serve as both the charge storage and connection node, since the spacial variation of carrier concentration is small. The fundamental semiconductor equations are then simplified using the nodal arrangement and transformed into the lumped-charge equations for each region.

III. The Lumped-Charge Diode Model

A typical one-dimensional (1-D) forward-biased on-state charge carrier distribution in a $P^+N^-N^+$ diode is shown in Fig. 1. Since the lightly doped N^- region stores the excess carriers, which determine the switching characteristics of the device, three nodes, indicated by 2, 3, and 4 in Fig. 2 are chosen for this region. Nodes 2 and 4 are connection nodes, and node 3 is a charge-storage node. Carriers in the heavily doped end regions do not penetrate deeply beyond the vicinity of the junctions. Hence, single-charge nodes 1 and 5 are sufficient for these regions. They are located at the depletion boundary of the end regions. They serve as both connection and charge-storage nodes.

The process for converting the six groups of the fundamental semiconductor and circuit equations to the lumped-charge equations using the nodal assignment is given next.

A. Current Density Equations

The 1-D equation [14] for hole current density is

$$j_p = qp\mu_p E - qD_p \frac{dp}{dx}. \tag{1}$$

Carrier (hole) transport between nodes 2 and 3 can be represented using the quantities shown in Fig. 2:

$$J_{p23} = q\frac{(p_2 + p_3)}{2}\mu_p \frac{v_{23}}{d_{23}} + qD_p \frac{p_2 - p_3}{d_{23}}. \tag{2}$$

Note that J_{p23} represents the hole current density between nodes 2 and 3. The first term on the right-hand side of (2) is the linearized drift term, and the second is the linearized diffusion term. Here, d_{23} is the distance between nodes 2 and 3. The averaged carrier concentration between nodes 2 and 3 is needed in the first term. For simplicity, the following approximation (3) is used:

$$\frac{p_2 + p_3}{2} \rightarrow p_3. \tag{3}$$

There can be several orders of magnitude difference between carrier concentrations at adjacent nodes. The term where this approximation is made is the drift term of the transport equation. The drift current is determined by the lowest carrier concentration in the region, and the higher concentrations are not so important. Thus, the approximation (3) is reasonable for forward conduction. In reverse recovery, the drift current is usually negligible. Typically, the accuracy loss by these approximations can be compensated by parameter extraction.

After multiplying and dividing (2) by the N^- region width d, the following is obtained:

$$J_{p23} = d \times qp_3 \frac{D_p}{\phi_t}\frac{v_{23}}{d \times d_{23}} + d \times qD_p \frac{p_2 - p_3}{d \times d_{23}} \tag{4}$$

where the thermal voltage $\phi_t = D_p/\mu_p$. A new parameter T_{p23} is defined as the approximate hole diffusion transit time

$$T_{p23} = \frac{d_{23} \times d}{D_p}. \tag{5}$$

The hole current equation in lumped-charge form can now be derived as

$$i_{p23} = A \times J_{p23} = \frac{q_{p3}}{T_{p23}}\frac{v_{23}}{\phi_t} + \frac{q_{p2} - q_{p3}}{T_{p23}} \tag{6}$$

where A is the device active area, $q_{p2} = qdAp_2$, and $q_{p3} = qdAp_3$. The magnitudes of these two charges have been normalized to the N^- region volume. Note that all charge quantities are normalized by multiplying by the metallurgical base volume.

At this point, the physical picture of the charge distribution in Fig. 2 can be abstracted in the standard lumped-charge nodal representation depicted in Fig. 3. Five lumped-charge nodes are sufficient to simplify the six groups of equations. The charge value at each node is proportional to the carrier concentration level. The hole current between nodes 3 and 4 in Fig. 3 is similar to (6) and can be directly written as

$$i_{p34} = \frac{q_{p3}}{T_{p34}}\frac{v_{34}}{\phi_t} + \frac{q_{p3} - q_{p4}}{T_{p34}} \tag{7}$$

where $q_{p4} = qdAp_4$ and T_{p34} is the approximate hole transit time between nodes 3 and 4. The electron currents (not shown in Fig. 3) can be derived in a similar manner.

B. Continuity Equations

The continuity equation [14] for holes is

$$\frac{\partial p}{\partial t} = G_p - U_p - \frac{1}{q}\nabla \cdot J_p. \tag{8}$$

The total charge in the N^- region can be approximated by q_{p3} at charge-storage node 3. Multiplying (8) by the electron

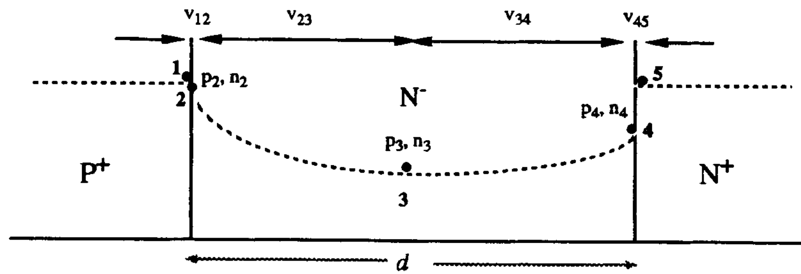


Fig. 2. Location of charge nodes in the $P^+N^-N^+$ diode structure. Electron and hole carrier concentration variables at each node and voltage drop along the device are also shown.

unit charge and base volume and rearranging give the lumped-charge form

$$i_{p23} - i_{p34} = \frac{q_{p3} - Q_{B_p}}{\tau_3} + \frac{dq_{p3}}{dt} \tag{9}$$

which is the well-known charge-control equation. The terms i_{p23} and i_{p34} represent the hole current flowing in and out of the N^- region and $Q_{B_p} = qAdp_{n0}$, the thermal equilibrium hole charge in the N^- base region. The first term on the right-hand side represents charge-carrier recombination and the second term charge variation with time. An averaged carrier lifetime τ_3 is used. The electron continuity equation for the N^- base region can be similarly derived.

No continuity equation is written for charges q_{p2} and q_{p4}, which are at the connection nodes 2 and 4. Only one charge node represents the total stored charge q_{p3} in the N^- base region. However, the effect of end-region recombination in the P^+ and N^+ regions is included by applying the continuity equation to nodes 1 and 5 in Fig. 3 [3].

C. Charge Neutrality Equations

The electron and hole charges are linked outside the junction-depletion regions by the neutrality equations. Since the dielectric relaxation time in a semiconductor material like silicon is on the scale of 1 ps, space-charge redistribution is assumed instantaneous. Therefore, the electron charges at different locations in the charge neutral N^- region are equal to the injected excess hole charges plus the ionized background doping charge Q_B:

$$q_{n2} = q_{p2} + Q_B \tag{10}$$

$$q_{n3} = q_{p3} + Q_B \tag{11}$$

$$q_{n4} = q_{p4} + Q_B \tag{12}$$

where $q_{n2} = qAdn_2, q_{n3} = qAdn_3, q_{n4} = qAdn_4$, and $Q_B = qAdn_{n0}$. Here, n_{n0} is the thermal equilibrium electron concentration of the N^- region. These electron charges are also normalized to the N^- region volume. These equations are valid over all ranges of operation.

D. Boltzmann Relations (p-n Junction Equations)

The carrier concentrations at the P^+N^- junction are related to the junction voltage v_{12} by

$$p_2 = p_{n0} \exp\left(\frac{v_{12}}{\phi_t}\right). \tag{13}$$

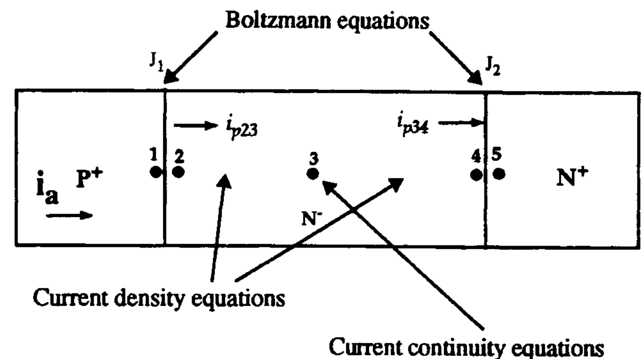


Fig. 3. Locations of the lumped-charge nodes and device equations in a 1-D $P^+N^-N^+$ diode structure.

Here, p_{n0} is the thermal equilibrium hole carrier concentration in the N^- region. Multiplication of the above expression by the N^- region volume gives

$$q_{p2} = Q_{B_p} \exp\left(\frac{v_{12}}{\phi_t}\right). \tag{14}$$

The charge at node 4 at the N^-N^+ junction in Fig. 3 is given in a similar manner to (14):

$$q_{n4} = Q_B \exp\left(\frac{v_{45}}{\phi_t}\right). \tag{15}$$

E. Poisson Equation [14]

The Poisson equation (16) is used to describe the effects of variation of junction-depletion width under reverse bias voltage:

$$-\frac{d^2v}{dx^2} = \frac{\rho(x)}{\varepsilon_s}. \tag{16}$$

Here, ε_s is the silicon dielectric constant and $\rho(x)$ the charge density. The depleted region of the P^+N^- junction extends significantly into the N^- region during reverse bias, squeezing the hole and electron charges into a smaller volume, as shown in Fig. 4. The positive charges in the depleted region consist of immobile ionized donors (n_{n0}) and holes (p_i) injected from the base. These holes are assumed to travel at saturation velocity v_{sat}:

$$|i_{p23}| = qAp_i v_{\text{sat}}. \tag{17}$$

Integrating (16) twice over the depleted region and rearranging terms gives

$$x_n = \left(\frac{2\varepsilon_s(\phi_{12} - v_{12})}{q\left(n_{n0} + \dfrac{|i_{p23}|}{qAv_{\text{sat}}}\right)} \right)^{1/2}. \tag{18}$$

Here, x_n is the depletion boundary and ϕ_{12} the built-in potential. The transit time T_{p23}, defined in (5), now becomes a variable, which depends upon $(d - x_n)$.

F. KCL and KVL

Kirchoff current laws (KCL's) and Kirchoff voltage laws (KVL's) are needed to link the device internal behavior to terminal characteristics. According to KCL, the terminal currents are equal to the sum of all the internal current components at each device cross section. According to KVL, the terminal voltages are equal to the sum of all the internal voltage drops along the device.

To ensure that the model equations are complete and solvable, the following checklist should be reviewed.

1) Are all the necessary charge equations included?
2) Are all equations unique (redundancy inspection)?
3) Are all current and voltage variables linked by internal charge variables?
4) Does the total number of independent equations agree with the total variable count? For a two-terminal device, the variable count should be one greater than the equation count; for a three-terminal device, the variable count should be two more than the equation count.

The complete set of diode model equations ready for implementation follows:

$$i_{p23} = \frac{q_{p2} - q_{p3}}{bT_n} + \frac{q_{p3}}{bT_n}\frac{v_{23}}{\phi_t} \tag{19}$$

$$i_{n23} = \frac{q_{p3} - q_{p2}}{T_n} + \frac{Q_B + q_{p3}}{T_n}\frac{v_{23}}{\phi_t} \tag{20}$$

$$i_{p34} = \frac{q_{p3} - q_{p4}}{bT_n} + \frac{q_{p3}}{bT_n}\frac{v_{34}}{\phi_t} \tag{21}$$

$$i_{n34} = \frac{q_{p4} - q_{p3}}{T_n} + \frac{Q_B + q_{p3}}{T_n}\frac{v_{34}}{\phi_t} \tag{22}$$

$$i_{n23} = \frac{1}{\tau_1}\left((q_{p2} + Q_B)\exp\left(\frac{v_{12} - \phi_{12}}{\phi_t}\right) - Q_{Pn}\right) \tag{23}$$

$$i_{p23} - i_{p34} = \frac{q_{p3} - Q_{Bp}}{\tau_3} + \frac{dq_{p3}}{dt} \tag{24}$$

$$i_{p34} = \frac{1}{\tau_5}\left(q_{p4}\exp\left(\frac{v_{45} - \phi_{45}}{\phi_t}\right) - Q_{Np}\right) \tag{25}$$

$$q_{p2} = Q_{Bp}\exp\left(\frac{v_{12}}{\phi_t}\right) \tag{26}$$

$$q_{p4} = Q_B\left(\exp\left(\frac{v_{45}}{\phi_t}\right) - 1\right) \tag{27}$$

$$l = \left(\frac{\phi_{12} - v_{12}}{\phi_B\left(1 + \dfrac{|i_{p23}|}{I_B}\right)} \right)^{1/2} \tag{28}$$

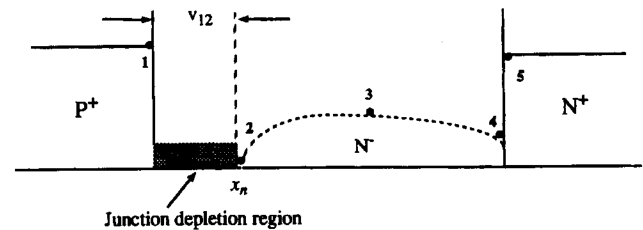


Fig. 4. Charge distribution in the P$^+$N$^-$ region during a reverse-recovery transient (the scale is relative).

$$T_n = T_{n0}(1 - l)^2 \tag{29}$$

$$v_{AK} = v_{12} + v_{23} + v_{34} + v_{45} \tag{30}$$

$$i_A = i_{n23} + i_{p23} \tag{31}$$

$$i_A = i_{n34} + i_{p34}. \tag{32}$$

Note that the neutrality equations (10)–(12) are used to eliminate the electron charges in the above model equations.

Equations (19)–(22) are electron and hole current equations between nodes 2 and 3 and nodes 3 and 4. Parameter b is the mobility ratio of electrons and holes. To further simplify the model for ease of parameter extraction and implementation, node 3 is assumed to be in the center of the base region. Thus, the transit times T_{p23} and T_{p34} become equal. Parameter T_n is the electron transit time and equal to T_{p23}/b.

Equation (23) combines the p-n junction equation at J_1 and the simplified continuity equation for node 1, where charge-storage effects are neglected due to the short carrier lifetime observed in the heavily doped P$^+$ end region. Equation (25) is similar to (23), but for J_2 and node 5 in the N$^+$ end region. Parameters τ_1 and τ_5 are equal to the products of minority carrier lifetimes in the end regions times the diffusion volume of the end regions divided by the base region volume. Parameters Q_{Pn} and Q_{Np} are the electron and hole background doping charges in the P$^+$ and N$^+$ regions, respectively. Since they have a negligible effect on the model, they are omitted in final implementation. Parameters ϕ_{12} and ϕ_{45} are the built-in potentials of the two junctions. Equation (24) is identical with (9).

Equations (26) and (27) are the p-n junction equations, identical with (14) and (15). Equations (28) and (29) account for the J_1 junction-depletion width variation effects, where the constant parameters $\phi_B = qn_{n0}d^2/2\varepsilon_s$ and $I_B = qAn_{n0}v_{\text{sat}}$. Equations (30)–(32) apply KVL and KCL to the model.

The P$^+$N$^-$ diffusion and depletion capacitances are both intrinsically built into the model. The diffusion capacitance is embedded in the charge transport equations, namely, current (19)–(22) and continuity (23)–(25). The depletion capacitance is embedded in the Poisson equations (28)–(29). The user can add additional capacitance, if needed, to account for overlap capacitance.

Breakdown and punchthrough effects are best modeled with separate empirical equations. These equations are omitted in this fundamental model.

IV. Model Analysis

Under most circumstances, the model equations can be solved directly for the dc current–voltage (I–V) characteristics

as well as for the turn-on and turn-off transients. These solutions can be used to verify the model and extract model parameters.

A. DC I–V Characteristics

The model equations can be solved at three distinct current levels: low-level injection, high-level injection without end-region recombination, and high-level injection dominated by end-region recombination.

The dc on-state I–V characteristic at low-level current injection is derived from (19)–(32), assuming $i_{n23}, i_{p34} = 0$, and $Q_B \gg q_{p3}$:

$$I_A = \frac{Q_{Bp}}{\tau_3 + bT_{n0}}\left[\exp\left(\frac{V_{AK}}{\phi_t}\right) - 1\right]. \quad (33)$$

At medium current levels, power diodes operate in high-level injection with insignificant end-region recombination. The I–V characteristic equation can be obtained from (19) to (32), assuming i_{n23} and i_{p34} are still negligible and $q_{p3} \gg Q_B$:

$$I_A = I_{SM}\exp\left(\frac{V_{AK}}{2\phi_t} - \frac{(b+1)T_{n0}}{4\tau_3}\right) \quad (34)$$

$$I_{SM} = \left[\frac{Q_{Bp}Q_B}{\left(\tau_3 + \frac{b}{2}T_{n0}\right)\left(\tau_3 + \frac{1}{2}T_{n0}\right)}\right]^{1/2}. \quad (35)$$

As current increases to higher levels, device operation enters the regime, where end-region recombination dominates. To derive the basic I–V relationship, end-region recombination is assumed to be symmetrical, with equal mobilities for electrons and holes. Then, models (23) and (26) can be combined to form (36); (25) and (27) are combined to form

$$i_{n23} = \frac{q_{p2}(q_{p2} + Q_B)}{\tau_E Q_E} \quad (36)$$

$$i_{p34} = \frac{q_{p4}(q_{p4} + Q_B)}{\tau_E Q_E}. \quad (37)$$

Here, $\tau_E = \tau_1 = \tau_5$ and Q_E represent the end-region charge defined as

$$Q_E = Q_B\exp\left(\frac{\phi_{45}}{\phi_t}\right) = Q_{Bp}\exp\left(\frac{\phi_{12}}{\phi_t}\right).$$

Since τ_E and Q_E always occur together in the model as $\tau_E Q_E$, they form a single emitter recombination parameter $E_r = \tau_E Q_E$. In model implementation, (36) and (37) are used to eliminate the junction built-in potentials ϕ_{12} and ϕ_{45} as model parameters.

Using (36) and (37) to replace (23) and (25), the model equations can be solved for the I–V characteristic for high-current operation under end-region recombination:

$$\frac{V_{AK}}{2\phi_t} = \ln\left(\frac{q_{p3}\left(1 + \frac{1}{2}\frac{T_{n0}}{\tau_3}\right)}{\sqrt{Q_{Bp}Q_B}}\right) + \frac{T_{n0}I_A}{q_{p3}} \quad (38)$$

where

$$q_{p3} = \tau_3 I_{E0}\left[\left(\frac{2I_A}{I_{E0}} + 1\right)^{1/2} - 1\right] \quad (39)$$

$$I_{E0} = \frac{E_r}{4(\tau_3 + \frac{1}{2}T_{n0})^2}. \quad (40)$$

Here, I_{E0} represents the I_A threshold for the onset of end-region recombination. Note that combining (38)–(40) under the condition $I_A \ll I_{E0}$ is identical to (34), with $b = 1$. Operation at $I_A \gg I_{E0}$ is so insensitive to the mobility ratio that the $b = 1$ approximation causes less than a 6% shift in I_A for constant V_{AK}. Equations (33), (34), and (38) closely approximate the standard p-i-n diode equations for operation under low-level, high-level, and end-region recombination conditions [16].

B. Transient Analysis

Forward recovery occurs due to conductivity modulation at initial turn-on. The diffusion capacitance predominates in this transient, and the depletion capacitance can be neglected. Current is assumed to increase linearly as $i_A = a_f t$, where a_f is the rate of current rise. Using (19)–(32) and setting (23) and (25) to zero, the forward recovery voltage waveform is derived

$$v_{AK} - v_j = \frac{2T_{n0}\phi_t(1+b)a_f t}{a_f\tau_3[t - \tau_3(1 - e^{-(t/\tau_3)})] + Q_B}. \quad (41)$$

Here, $v_j = v_{12} + v_{45}$ is the forward bias junction voltage, and $v_{AK} - v_j$ is the voltage drop in the base. The forward recovery time t_{fr} is the time the voltage takes to rise from its on-state to peak value. The forward recovery time for $t_{fr} \ll \tau_3$ can be found by differentiating (41) and setting the result to zero:

$$t_{fr} = \sqrt{\frac{Q_B}{a_f}}. \quad (42)$$

The peak forward voltage $V_{fr} = v_{AK}(t_{fr})$:

$$V_{fr} = 2T_{n0}\phi_t(1+b)\left(\frac{a_f}{Q_B}\right)^{1/2} + v_j. \quad (43)$$

Note that V_{fr} increases with a wider base, lighter base doping, and a higher rate of current rise.

Power diodes are normally turned off with inductive loads, which produce the turn-off current waveform shown in Fig. 5. The voltage dependence of the transit time $T_n(l)$ is important, as indicated by (28) and (29).

For $0 \le t \le T_1$, the internal stored charge q_{p3} can be determined using (24) under the circuit condition $i_A(t) = I_F - a_r t$ and neglecting end-region recombination (assuming i_{n23} and $i_{p34} = 0$):

$$q_{p3}(t) = a_r\tau_3\left(T_0 + \tau_3 - t - \tau_3\exp\left(-\frac{t}{\tau_3}\right)\right). \quad (44)$$

At time $t = T_1$, v_{12} becomes reverse-biased and $q_{p2} \approx 0$. From (19) and (20), q_{p3} can be found:

$$q_{p3}(T_1) = \frac{b}{n}I_{RM}T_n. \quad (45)$$

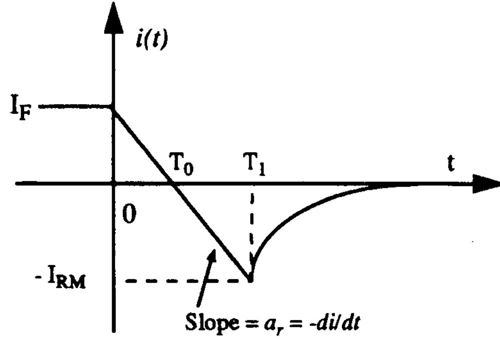


Fig. 5. A diode reverse-recovery current waveform.

Here, parameter $n = 2$. For $t \geq T_1$, (19), (20), (24), and the charge neutrality equations give

$$-i_A(t) = \frac{nq_{p3}}{T_n} = I_{RM} \exp\left(-\frac{t - T_1}{\tau_{rr}}\right) \tag{46}$$

where

$$\frac{1}{\tau_{rr}} = \frac{n}{bT_n} + \frac{1}{\tau_3}. \tag{47}$$

The parameter τ_{rr} is the voltage-dependent reverse-recovery time constant. The parameter τ_{rr} can be approximately considered as a constant only when the diode is turned off at low reverse voltage, for instance, 10% of its breakdown voltage. In this case, T_n is equal to T_{n0}. The factor n is added so that (45)–(47) can be valid for either low-level ($n = 1$) or high-level ($n = 2$) injection conditions. Most power diodes turn off under high-level injection, but the final current (tail current) flows under conditions of low-level injection with a longer time constant.

Note that the complete model does include the dynamic effects of end-region recombination on reverse-recovery waveforms. Experimentally, this effect is observed as a decrease in effective diode lifetime at high currents.

V. Parameter Extraction

A major advantage of lumped-charge models is that most of the model parameters can be extracted from simple dc and transient measurements. The eight model parameters for the lumped-charge power diode model are:

1) electron transit time: T_{n0};
2) lifetime: τ_3;
3) thermal equilibrium electron and hole charges in the base: Q_B and Q_{Bp};
4) symmetric end-region recombination parameter: E_r;
5) voltage-dependent reverse-recovery parameters: ϕ_B and I_B;
6) mobility ratio of electrons and holes: b.

First, a reverse-recovery measurement at low voltage (less than 10% of the diode breakdown voltage) is required. An expression with only one unknown parameter τ_3 can be obtained by setting $t = T_1$ in (44), eliminating q_{p3} using (45), then eliminating T_0 using $T_0 = T_1 - I_{RM}/a_r$:

$$I_{RM} = a_r(\tau_3 - \tau_{rr})\left[1 - \exp\left(-\frac{T_1}{\tau_3}\right)\right]. \tag{48}$$

TABLE I
Parameter Extraction of the Diode Model

Measurements	Parameters	Equations
Reverse recovery	τ_3, T_{n0}	(47), (48)
Forward recovery	Q_B, T_{n0}	(42), (43)
dc low-level I-V	Q_{Bp}	(33)
dc high-level I-V	E_r	(38), (39), (40)
None	ϕ_B, I_B	(49) - (52)

The reverse-recovery time constant τ_{rr} can be measured from the recovery curve. After τ_3 is extracted from (48), T_{n0} is calculated from (47).

The diode base volume Vol_B can be estimated:

$$Vol_B = \frac{\sqrt{Q_B Q_{Bp}}}{qn_i}. \tag{49}$$

Diode basewidth d can be approximated using the electron version of the transit time equation similar to (5), assuming d_{23} is half of the basewidth d:

$$d = \sqrt{2T_{n0}D_n}. \tag{50}$$

Here, D_n is the electron diffusion constant. The device active area of the diode can also be estimated by $A = Vol_B/d$. The base background doping can then be calculated by $n_{n0} = Q_B/qVol_B$. Therefore, parameters ϕ_B and I_B can be calculated:

$$\phi_B = \frac{qn_{n0}\, d^2}{2\varepsilon_s} \tag{51}$$

$$I_B = qAn_{n0}v_s. \tag{52}$$

Note that this indirect method only provides approximate values for ϕ_B and I_B, since these parameters are not calculated from the reverse-recovery transient. Thus, some adjustments in these parameters will be needed for the best model performance. The mobility ratio b has a minor effect on external characteristics. This parameter can be used to adjust for differences in the transit time T_{n0} values calculated from forward and low-voltage reverse recoveries or it can be simply set to its silicon value $b = 3$. If forward recovery data is not available, the base charge Q_B can alternatively be determined from (34).

A summary of extraction of the model parameters from the measurements is given in Table I. For power integrated circuit (IC) design, parameters need to be based upon process information. Since this diode model is physics-based, an alternative set of process-based parameters could be defined.

VI. Sample Results

The model is implemented in the SABER circuit simulator and tested under dc and transient conditions. The simulated dc I–V characteristics are compared with the data book values

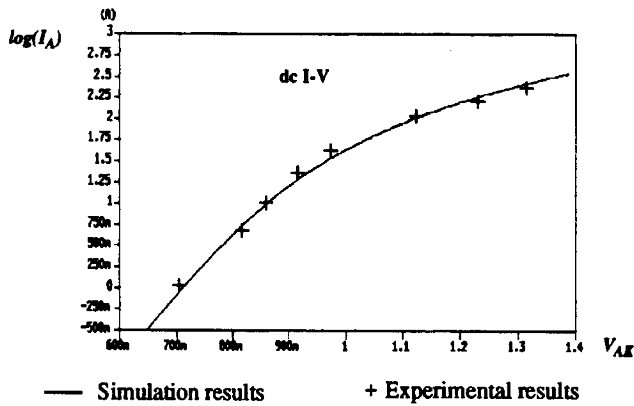


Fig. 6. DC I-V characteristics comparing the diode model with a Motorola MR754 diode. Note that the vertical scale is $\log_{10}$.

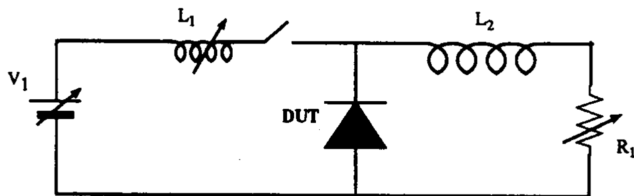


Fig. 7. A test circuit for measuring diode switching characteristics.

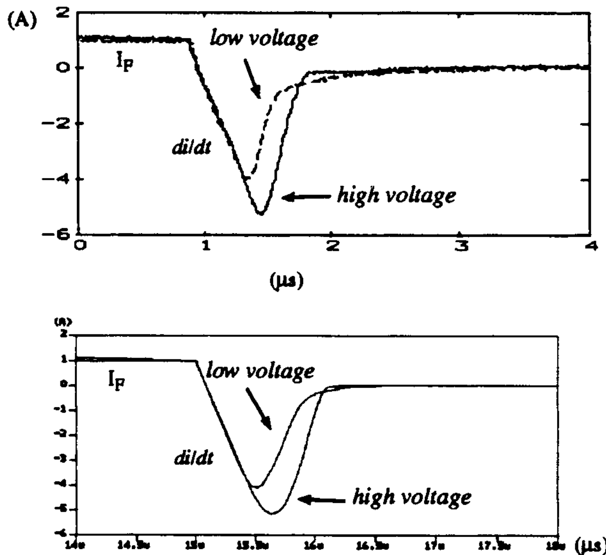


Fig. 8. Measured (upper) and simulated (lower) reverse-recovery current waveforms of MR852 under low and high reverse voltages.

for a Motorola MR754 diode in Fig. 6. Note that the transition from low to high current is smooth.

A Motorola diode (MR852) is measured using the reverse-recovery test circuit shown in Fig. 7. Two measurements were performed at low and high reverse voltages to observe the voltage dependence of reverse recovery with identical forward current and di/dt. Fig. 8 shows measured and simulated reverse-recovery current waveforms. Fig. 9 shows the voltage waveforms. Note that both simulated and measured data show the presence of the tail current at low voltage and absence at high voltage.

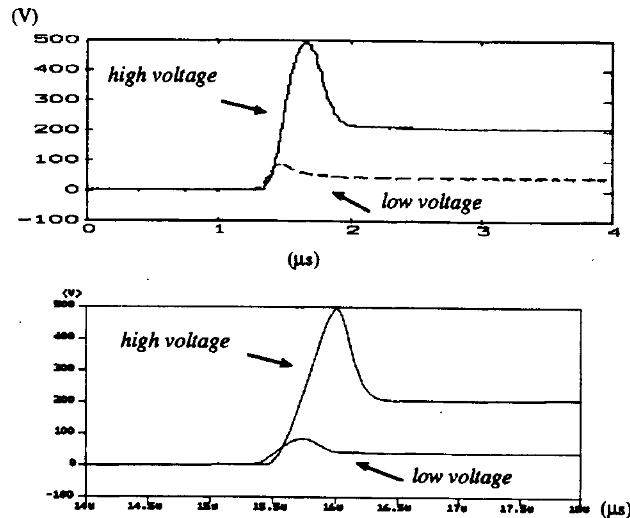


Fig. 9. Measured (upper) and simulated (lower) reverse-recovery voltage waveforms of MR852 at low and high reverse voltages.

VII. Discussion

This diode model adds several features to the older lumped-charge diode models [1], [3]. Low-level operation and voltage-dependent switching are included to add tail current effects. Although, the number of model equations is increased, the 1-D physical structure is retained. Low- and high-level injection effects and nonquasi-static effects are inherently built-in. Since the model is based on device physics, one can observe internal physical quantities like voltages, currents, and charge distributions under different circuit conditions through simulation. Additional effects, such as Auger recombination, carrier–carrier scattering, and thermal effects could be added to the model due to its physics-based nature.

Model accuracy can be improved through increasing the number of the lumped-charge nodes, but model complexity then increases undesirably.

The equations can be rearranged in a form sufficiently simple to simulate most electrical measurements, such as dc I–V characteristics and turn-on and turn-off transients. Parameters can be extracted by comparing these simplified equations with measured quantities. By determining all the parameters from measurements on packaged devices, adjustments made for the approximations used in the modeling process are compensated.

The primary approximation of this approach is linearization of charge carrier distribution in each region.

VIII. Conclusion

The lumped-charge modeling technique represents a systematic approach for model development of power semiconductor devices. The power diode model developed here provides superior performance in accuracy and computational speed. By following this foundation, all other power bipolar semiconductor devices are relatively easy to construct.

References

[1] C. L. Ma and P. O. Lauritzen, "A simple power diode model with forward and reverse recovery," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 342–346, 1993.

[2] R. Kraus, K. Hoffmann, and H. J. Mattausch, "A precise model for the transient characteristics of power diodes," in *Proc. IEEE Power Electronics Specialists Conf.*, 1992, pp. 863–869.
[3] C. L. Ma, P. O. Lauritzen, and P. Y. Lin, "A physically-based lumped-charge P-ν-N diode model," in *Proc. European Power Electronics Conf.*, Brighton, England, 1993, pp. 23–28.
[4] A. Strollo, "A new SPICE subcircuit model of power P-I-N diode," *IEEE Trans. Power Electron.*, vol. 9, no. 6, pp. 553–559, 1994.
[5] H. Göbel, "A unified method of modeling semiconductor power devices," *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 497–505, 1994.
[6] D. Metzner, T. Vogler, and D. Schroeder, "A modular concept for the circuit simulation of bipolar power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 9, no. 5, pp. 506–513, 1994.
[7] C. L. Ma *et al.*, "A systematic approach to modeling power semiconductor devices based on charge control principles," in *Proc. IEEE Power Electronics Specialists Conf.*, Taiwan, 1994, pp. 31–37.
[8] C. L. Ma, "Modeling of power bipolar semiconductor devices," Ph.D. dissertation, Univ. Washington, Seattle, WA, 1994.[1]
[9] C. L. Ma, P. O. Lauritzen, and J. Sigg, "Modeling of high-power thyristors using the lumped-charge modeling technique," in *6th European Conf. on Power Electronics and Applications*, Spain, 1995.
[10] ——, "A physics-based GTO model for circuit simulation," in *IEEE Power Electronics Specialists Conf.*, Atlanta, GA, 1995, pp. 872–878.
[11] Z. Hossain *et al.*, "A physics-based MCT model using the lumped-charge modeling technique," in *IEEE Power Electronics Specialists Conf.*, Baveno, Italy, 1996, pp. 23–28.
[12] I. Budihardjo and P. O. Lauritzen, "The lumped-charge Power MOSFET model, including parameter extraction," *IEEE Trans. Power Electron.*, vol. 10, no. 3, 1995, pp. 379–387.
[13] I. Budihardjo, P. O. Lauritzen, and C. Xu, "Simulation of high frequency PWM and quasi-resonant converters using the lumped-charge power MOSFET model," in *Proc. IEEE APEC*, 1994, pp. 1042–1048.
[14] S. M. Sze, *Physics of Semiconductor Devices*. New York: Wiley, 1981.
[15] G. Massobrio and P. Antognetti, *Semiconductor Device Modeling with SPICE*, 2nd ed. New York: McGraw-Hill, 1993.
[16] J. Baliga, *Power Semiconductor Devices*. Boston, MA: PWS, 1995.

Cliff L. Ma (S'90–M'94) was born in Beijing, China, on September 23, 1964. He received the B.S. degree from California State University, Fresno, and the M.S. and Ph.D. degrees from the University of Washington, Seattle, all in electrical engineering, in 1989, 1991, and 1994, respectively.

He worked at Siemens Corporate R&D in Munich, Germany, in the summers during his Ph.D. program. He was appointed as an Instructor teaching undergraduate classes at the University of Washington in 1993. He joined Analogy, Inc., Beaverton, OR, in 1994 as a Senior Engineer. He is responsible for device modeling research and development at Analogy.

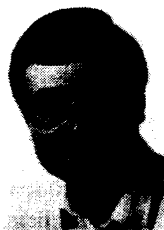
Dr. Ma currently serves in professional activities as an IEEE Transactions Reviewer and an IEEE Conference Committee Member. He received the Siemens Fellowship for power semiconductor device modeling.

[1] This dissertation can be ordered through: UMI, 300 North Zeeb Road, Ann Arbor, MI 48103 USA. UMI Number: 9523719. Telephone: 1-800-521-0600.

Peter O. Lauritzen (S'58–M'62–SM'88) was born in Valparaiso, IN, on February 14, 1935. He received the B.S. degree from the California Institute of Technology, Pasadena, and the M.S. and Ph.D. degrees from Stanford University, Stanford, CA, all in electrical engineering, in 1956, 1958, and 1961, respectively.

From 1961 to 1965, he worked on semiconductor device research and development at Fairchild Semiconductor Division, Palo Alto, CA. From 1965 to 1978, he was on the Electrical Engineering Faculty at the University of Washington, Seattle, where his research activities included semiconductor device noise, radiation effects, operation at cryogenic temperatures, and instrumentation. During 1979 and 1980, he was Engineering Manager of Avtech Corporation, Seattle. He returned to the University of Washington in 1981, where he teaches courses on power electronic circuits and devices and conducts research on power electronic device modeling. He is currently a Professor of Electrical Engineering and Co-Director of the NSF-CDADIC University-Industry Center.

Dr. Lauritzen was Conference Chair for IEEE PESC '93. He is currently on the IEEE PELS Technical Committee on Computers in Power Electronics. He is a Registered Professional Engineer in the state of Washington.



Jakob Sigg was born in Trochtelfingen, Germany, on May 1, 1955. He received the Diploma degree in physics in 1983 from the University of Heidelberg, Heidelberg, Germany, and the Ph.D. degree in physics from the University of Stuttgart, Stuttgart, Germany, in 1987.

From 1984 to 1987, he was with the Max-Planck-Institute for Solid State Research, Stuttgart, working on the coherence properties of semiconductor lasers. In 1987, he joined the Corporate Research and Development Laboratories of Siemens AG, Munich, Germany. From 1987 to 1992, he was engaged in the characterization and modeling of laser diodes and the study of optical feedback effects. Since 1993, he has been with the Department of Power Electronics, Siemens AG, working on the modeling of power electronic devices.

Dr. Sigg is a Member of the German Physical Society.