

# A Row-Column Summing Readout Architecture for SiPM based PET Imaging Systems

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**Abstract**— Recent developments in the area of Positron Emission Tomography (PET) detectors using Silicon Photomultipliers (SiPMs) have demonstrated the feasibility of higher resolution PET scanners due to a significant reduction in the detector form factor. However, reduced size implies a corresponding increase in the detector density, resulting in a proportional rise in the number of channels interfacing a SiPM array with the digital backend. This paper explores a row-column-diagonal decoding architecture to simplify and reduce the required channels between the individual elements in the SiPM array, and the backend digital electronics. Accumulation of noise presents itself as a challenge to the row-column summation architecture. This may lead to an increased chance of false triggering as compared to a more traditional approach with dedicated single-channel readout for each individual SiPM. This work explores various circuit implementation approaches for threshold detection as applied to front-end electronics, which minimizes the accumulation of dark noise, and reduces the possibility of a false triggering event. Current comparator topologies are explored in the context of fastest turn-on time and the impact of realizing these threshold detection techniques in the context of our row-column summation architecture. The proposed readout electronics is currently being realized in STMicroelectronics 130 nm CMOS process.

## I. INTRODUCTION

THE recent realization of Silicon Photomultiplier (SiPM) devices as solid-state detectors for Positron Emission Tomography (PET) holds the promise of miniaturized PET scanners. These SiPM devices feature a detector vastly smaller in size as compared to bulky vacuum photomultiplier tubes (PMT), which enables a denser detector array, promising higher resolution PET images. In addition, SiPM devices have higher quantum efficiency, higher gain, operate at lower bias voltages, are insensitive to magnetic fields, and provide excellent timing resolution, all of which are characteristics favorable for Magnetic Resonance Imaging (MRI) applications. In addition, this technology facilitates the interconnection between the detector and the read-out electronics.

SiPM devices have been implemented in CMOS technology in recent years, thus potentially enabling integration of a significant portion of the interface electronics on the same substrate with the detectors, which would reduce interconnect parasitics, and lower power consumption. With respect to readout channels for SiPM detectors in PET applications, a majority of the circuits have been derived from previous discrete or integrated implementations developed for PMTs [1-3]. In contrast, recent efforts have attempted to integrate the readout electronics on a single die with dedicated designs for use with SiPM detectors [4-6]. However, a number of challenges exist for highly integrated front-end detectors. Specifically, the reduced size of the SiPM devices compared to PMTs implies an increase in the detector density, resulting in a proportional rise in the number of read out channels which interface to the digital backend. With the advent of 3D positioning architectures, X, Y, and Z components of an event can be captured, improving both spatial and image resolution. However, 3D positioning architectures lead to further increase in the array density, and hence the number of read channels also grows proportionally, requiring significantly more amplifiers and Analog-to-Digital Converters (ADC). In an effort to reduce the number of channels for high-element arrays, multiplexing techniques have been utilized, however this is done at the cost of losing spatial information. This paper describes an architecture which attempts to reduce the number of readout channels for highly dense SiPM arrays, while recovering all X, Y, and Z, spatial and timing information. This approach uses a row-column summing architecture (RCA), analogous to decoding methods used in digital memory arrays. This effectively reduces the number of channels from  $N^2$  to  $2N$ , for an  $N$  by  $N$  SiPM array. The row and column channels convey information about the position of a detected event. In addition, a single high-speed channel is used to extract timing information for all elements in the SiPM array. This reduces the number of high-speed ADCs from  $N^2$  to a single channel which captures the timing information, while the required Nyquist frequency of the  $2N$  row and column ADCs is significantly lower as compared to the bandwidth required of converters used in traditional interface electronics where each detector has a dedicated channel.

Although the RCA reduces the number of channels in an array, there are challenges introduced by this approach. Mainly, the accumulation of dark noise generated by all the SiPM devices along a given row or column channel may lead to falsely triggering an event. This work makes use of threshold detection circuitry to minimize the impact of dark noise current events. .

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Manuscript received November 15, 2013. This work was supported in part by NIH NIBIB EB001563, NIH NIBIB EB002117, NIH NCI CA136569, DOE DE-FG02-05ER15709, and Zecotek Photonics.

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The threshold detection circuitry runs in parallel to the main signal path which contains a current amplifier at the input, a wide band transimpedance amplifier which also performs a single-ended to differential conversion, and a programmable line driver. These components are realized in 130 nm STMicroelectronics HCMOS9GP process.

This paper begins with a discussion of the Row-Column architecture (RCA) for an N by N SiPM array, followed by a section on the threshold detection circuit. A discussion is then given on the challenges and strategies for realizing the high speed current comparator. A description is then given of the channel signal path. Lastly, some extracted simulation results are given for an ASIC design currently in fabrication using a 1.2 V 130 nm process.

## II. ROW COLUMN ARCHITECTURE (RCA)

Conventional readout electronics will dedicate an individual channel for each SiPM device in the array. Each channel consists of a SiPM detector which feeds either a current amplifier or transimpedance amplifier after which the signal is driven off chip into a cable connected between the readout electronics and the ADC at the backend where digital signal processing takes place. For an N by N array, the channels are replicated  $N^2$  times.

In the RCA approach, shown in Fig 1, each SiPM detector output feeds a low-input impedance programmable gain current amplifier. The amplifier interface is the only component of the readout electronics which is unique to each SiPM detector. The current amplifier has three output stages which feed a row output line, column output line and common pickoff line.

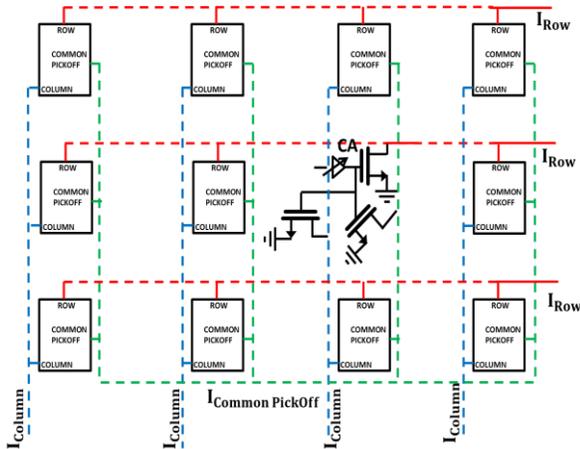


Fig 1. Row Column Summation Architecture

The row and column channels provide spatial information of a detected event. The common pickoff channel, used as the timing channel, sums the output of all the array elements. This allows better timing information with respect to any individual SiPM event in the array, since it reflects the total current drawn by the array when multiple elements are fired. As all SiPM elements share this channel and the intent is to optimize timing, this particular channel needs significantly higher

bandwidth as compared to the individual row and column readout (spatial positioning) channels. If there is a SiPM current at the input of any array element, there will be outputs across the corresponding row and column channels, as well as the common pickoff channel.

Each array element is implemented with a high speed current amplifier interfaced to the off chip SiPM device. The use of current amplifiers is motivated by the need to present low impedance from the perspective of the SiPM output, which reduces the current division between the amplifier input and the remaining SiPM cells. In addition, current mode circuits have significantly higher bandwidth compared to their voltage mode counterparts, thus facilitating wideband implementations. The use of a single amplifier to interface the SiPM device has the additional benefit of reducing cross talk between the SiPM devices in the array. In addition, because a single amplifier (rather than three) is used to supply a row, column, and pickoff signaling, the capacitance loading on the SiPM's cathode is minimized, further increasing the bandwidth of the detector-channel interface.

## III. THRESHOLD DETECTION

One challenge associated with the row-column summation approach is the potential accumulation of noise down a single line. This problem is exacerbated by combining the output of multiple SiPM devices along a row or column. The situation is illustrated in Fig 4, where the dark current generated in an individual SiPM device is shown to accumulate with other detectors, sharing a row or column output line. When the noise is added at the output, there is an increased chance of false triggering as compared to a single-channel readout of individual SiPMs, as the accumulated noise from the row or column output, is likely to be comparable to a desired signal; fig. 2.

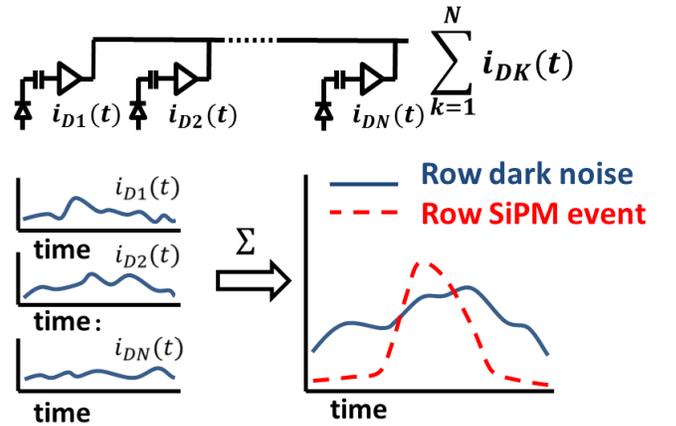


Fig 2. Dark Noise accumulation along a single row

In the RCA, threshold detection is used to decrease the noise contribution on the summation lines. The input SiPM current is compared with a programmable threshold current, and if the current of the input signal falls below a threshold which would signify a detected gamma event, the output stage of the current amplifier is disconnected from the summation

lines using the switches, as shown in Fig 3. Threshold detection becomes challenging for a continuous-time amplifier where the delay associated with the main amplifier and the threshold detection circuitry becomes critical. In short, any mismatch in the delay between these two paths will clip the rising edge of the SiPM pulse. Thus, the speed of the threshold detection circuitry becomes paramount to minimize any loss of information on a real detection event.

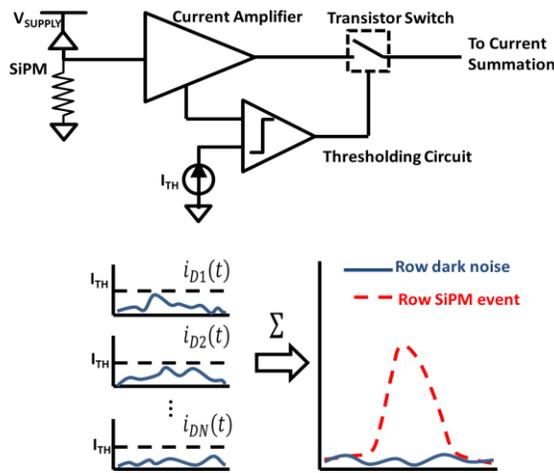


Fig 3. Threshold detection circuit

The signal is run current mode from the SiPM output to the row and column lines. As such, a current comparator is utilized to realize the threshold detection circuitry. Because current-mode signals are used, the input impedance of the comparator needs to be low to improve the bandwidth and minimize loading of the previous stage. In addition, to ensure all devices in the comparator remain in saturation, an input bias voltage is established at half the supply voltage. In the proposed current comparator, Fig. 4, the input stage utilizes a regulated cascode (transistors M1 – M5) to lower the input impedance of the circuit and reduce the propagation delay at high frequencies. An inverter chain at the output of the comparator, amplifies the threshold detection signal forcing it to run rail-to-rail. The inverter with resistive feedback (M6-M7) allows the transistors to operate in the saturation region, thus having a very high voltage gain. A replica bias circuit is implemented to force the DC bias voltage at the input of the CMOS inverters to  $V_{DD}/2$ . This further improves the propagation delay by holding the inverter input bias voltage to the tripping point of the comparator. The replica bias circuit also provides a resistive load which is better controlled over process, voltage and temperature (PVT) variations.

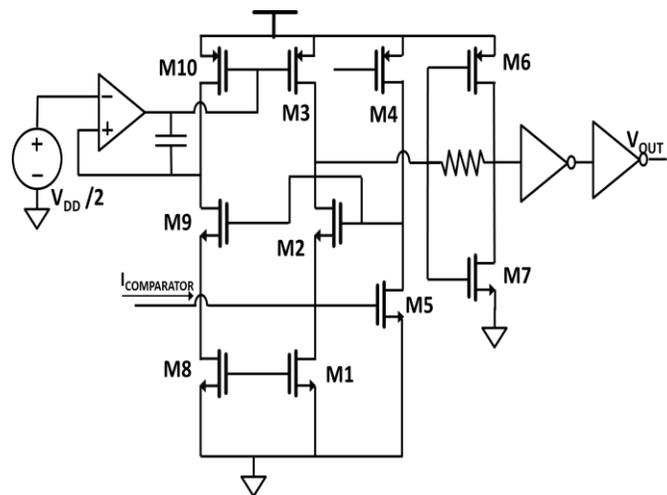


Fig 4. Current Comparator Schematic.

To minimize the propagation delay introduced by this threshold detection technique, a current-mode switching circuit is used which is analogous to high-speed current commuting mixers. The output stage of the current amplifier in the main signal path is either routed to the common row-column line, or to the supply when sitting idle. If an event is detected which is above the threshold current setting, the detection circuitry will current commute the amplifier's output stage into the common row-column line. This ensures that a constant bias current flows through the amplifier output stage, to allow for fast switching. Switching speeds up to 200ps, were simulated on the extracted layout.

#### IV. CHANNEL CIRCUIT IMPLEMENTATION

A single channel of the analog front-end electronics is shown in Fig. 5. A low input impedance regulated cascode current amplifier interfaces the SiPM device. A variable gain stage, at the output of the current amplifier, comprised of the current mirrors is used to modulate the gain of any array element independently. This is done to calibrate the gain mismatch between various SiPM devices in the array. The current mirrors at the output stage of the current amplifier are summed with the current from other amplifiers attached to a row, column or common pickoff path. A two stage cascode operational amplifier is used as the transimpedance amplifier to convert the single-ended summed current into a differential voltage. A differential interface is used to allow compatibility with the ADCs in the Phase II MiCES FPGA data acquisition [8] boards currently under development at the University of Washington. The signal is then driven off-chip using programmable analog line drivers which tune the driver output impedance to match the impedance seen looking into the cables which connect this chip to discrete ADCs and our Phase II MiCES FPGA. The line driver is tunable over a range of  $50\Omega - 200\Omega$  which compensates for a variation in the cabling length, shape, and differences in board loading effects.

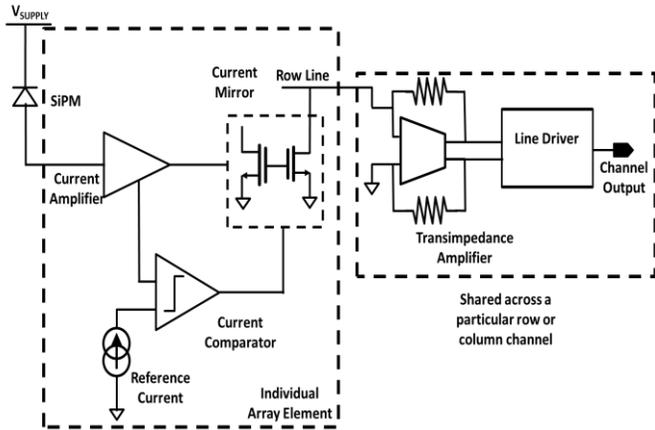


Fig.5. Block-level diagram of the Analog Front End

## V. RESULTS

This ASIC was designed and laid out in a 130 nm STMicroelectronics HCMOS9GP process. Extracted simulations were carried out using Cadence Spectre tools. The stand-alone current comparator was simulated by applying a square current pulse to the input. The time necessary to enable the main current amplifier was then measured to understand the speed of the threshold detection circuit. Under these simulation conditions, the propagation delay from the input current to the output voltage was found to be 300 ps, Fig. 6.

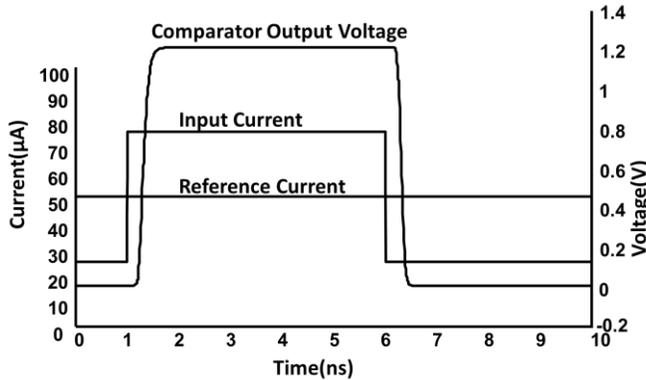


Fig. 6. Simulated propagation delay of current comparator with a current pulse applied to the threshold detection circuitry.

The impact of the comparator on the propagation delay of the channel, and the response of the channel to a square current pulse were also simulated. Without the comparator enabled, the delay from the input to the current summation node was 500ps. With the comparator enabled, the delay increased to 750 ps, Fig. 7. A switching transient is shown. However, this is at a significantly higher frequency relative to the bandwidth of the channel, and the desired detected signal.

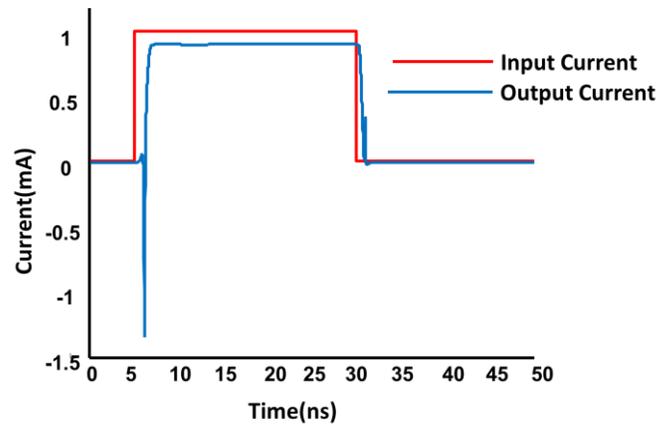


Fig. 7. Propagation delay across channel

To evaluate the performance of the entire system, a set of measured SiPM pulses taken from a Zecotek Photonics MAPD-3N1 using a 511 keV Ge-68 radiation source are used as input to the system, as shown in Fig 8. The differential voltage at the output of the channel shows the linearity and the bandwidth of the readout electronics is sufficient to accurately capture a SiPM pulse event.

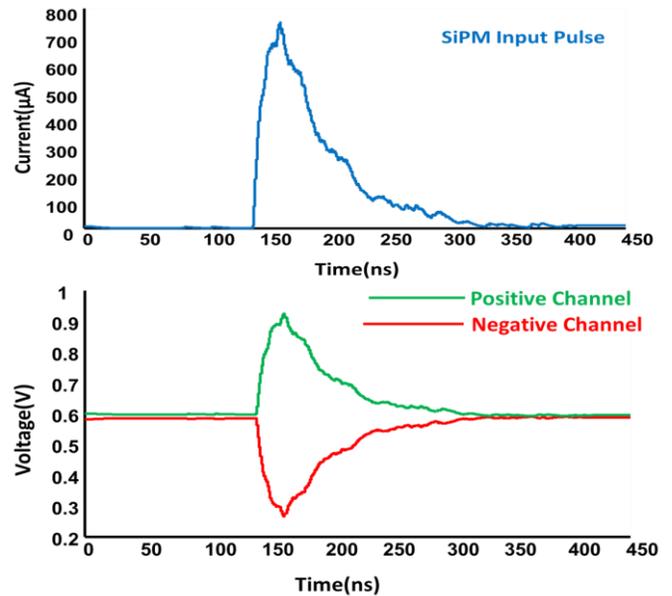


Fig. 8. Full-Channel Simulation using a measured SiPM pulse as an input source to the readout electronics.

A summary of the ASIC with its overall performance is given in the table below.

Table I Summary Results

Detector Module	LYSO/SiPM
Applications	Pre-Clinical and Organ specific PET
Process	STMicroelectronics 1.2 V 130nm
Die Size	3.9mm X 3.6mm
SiPM cells	64
Output Channels	16 + 1(common pickoff)
Power Consumption	30 mW/channel
Bandwidth	500 MHz
Transimpedance Gain	500 V/A

## VI. CONCLUSION

This work presents the design of a new front-end readout ASIC dedicated to PET imaging systems which facilitates the integration of the SiPM with the front end electronics. The Row Column architecture (RCA) reduces the number of channels between the SiPM array and the backend digital signal processing. Over the coming months, the ASIC described in this paper will be measured in the lab. In addition, we will design data acquisition boards which interface the CMOS front-end chip with the ADCs and the Phase II FPGA. . Our program seeks to eventually integrate the RCA design with on chip digitizing of the signals and a compact package to allow it to be tightly coupled to SiPM array elements with techniques such as bump bonding.

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