CrtSmile: A CAD Tool for CMOS RF Transistor Substrate Modeling Incorporating Layout Effects

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Abstract: This paper presents a new CAD tool *CrtSmile*, which automatically incorporates transistor layout effects for CMOS RF transistor modeling with an emphasis on substrate resistance extraction. The RF transistor layouts in the CIF/GDSII format are used to generate a layout dependent substrate model that can be included as a subcircuit with the BSIM3 device model. To support multi-finger RF transistor layout/bulk recognition, a pattern based layout extraction method is presented. *CrtSmile* incorporates a scalable substrate model for multi-finger transistors, which is dependent on transistor layout/bulk patterns and geometric layout information, such as the number of gate fingers, finger width, channel length, and bulk contact locations. This model is simple to extract and gives good agreement with the measured data for a 0.35µm CMOS process. A low noise amplifier design is evaluated with the new layout dependent substrate model and the proposed tool, showing the importance of CMOS RF transistor layout on substrate resistance modeling.

1. Introduction

At Giga hertz frequencies, non-quasi-static channel effects and the distributed nature of the gate and the substrate should be correctly modeled to accurately predict the MOS transistor behavior. Further, the scalability, accuracy and efficiency are three important factors in choosing the model. The influence of the substrate on MOS transistor performance has been studied in [1][5][8][10] where substrate effects have been incorporated into standard device models by attaching an external resistance network. BSIM4 [2] further applies a complex internal five-resistor substrate network to model the substrate. It has been shown that the simple one-resistor substrate network in [1] (Fig. 1) is accurate up to 10 Ghz and the substrate resistance is weakly dependent on biasing conditions [11].

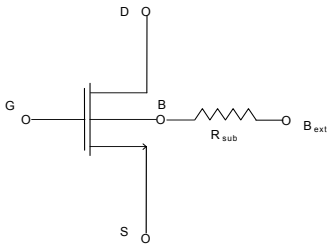

Figure 1. RF MOS transistor substrate network model of [1].

Previous work in substrate modeling is not sufficient for high frequency RF applications since transistor layout effects are not properly modeled. In general, RF transistors are realized by different kinds of multi-finger layout patterns and substrate contact locations to reduce parasitic effects and the layout areas. For example, Figs. 2(a) and 2(b) show two standard multi-finger transistors with different bulk contact patterns. In Fig. 2(a), the direction of bulk contacts is perpendicular to the finger direction. In Fig. 2(b), the direction of bulk contacts is parallel to the finger direction. Even though these two transistors have the same device size, their substrate resistances are different due to their different bulk contact patterns. The layout dependence of substrate resistance will become even severe for an interleaving multi-finger layout pattern as shown in Fig. 2(c) since the substrate is shared by two interleaving transistors. Therefore, a substrate model that does not consider multi-finger layout/bulk patterns will lead to incorrect results.

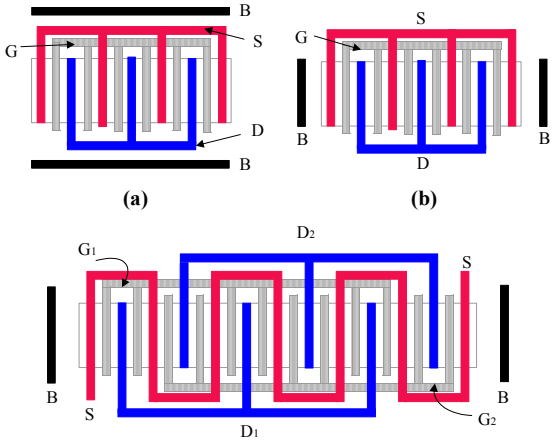

Figure 2. (a) Standard multi-finger transistor layout with perpendicular bulk contacts. (b) Standard multi-finger transistor layout with parallel bulk contacts. (c) Interleaving multi-finger transistor layout with parallel bulk contacts.

In addition to layout/bulk patterns, the substrate resistance is also dependent on geometric layout information, such as the number of fingers, finger width, channel length, bulk contact locations, etc. Recently [4][11] have proposed scalable substrate resistance models. In this paper, we present a new CAD tool *CrtSmile* (*C*MOS *R*F *T*ransistor *S*ubstrate *M*odeling *I*ncorporating *L*ayout *E*ffects), which automatically extracts layout/bulk patterns and geometric layout information from input layout files and accordingly generates layout dependent substrate models. A new scalable layout dependent substrate model based on [1] for different layout/bulk patterns and geometric layout parameters is also incorporated.

This paper is organized as follows. Section 2 introduces the system architecture of *CrtSmile*. The pattern based RF transistor layout extraction method is discussed in Section 3. Section 4 presents a scalable layout dependent substrate model. Measurement data on substrate resistance and a low noise amplifier example are shown in Section 5. Finally, Section 6 concludes this paper.

2. System architecture

The system architecture of *CrtSmile* is shown in Fig. 3. It can be used for both post-layout verification and pre-layout design.

During post-layout verification, a key task for layout extraction is to provide all the required geometric layout information as well as the layout/bulk pattern styles for the next step of substrate model generation. Therefore, a pattern based layout extraction program is developed with input layout files in the CIF/GDSII format. After the layout/bulk pattern and the geometric layout information are extracted, the layout dependent substrate model generation module is called and the final substrate resistance is calculated. For a pre-layout design, users should specify the candidate layout/bulk pattern style and all the required geometric layout parameters.

After the layout dependent substrate model generation, a behavioral substrate model is generated with geometric parameters as inputs instead of a specified substrate resistance value. The behavioral substrate model is realized with a sub-circuit in a SPICE-like simulator and attached to the BSIM3 device model for RF circuit design and optimization.

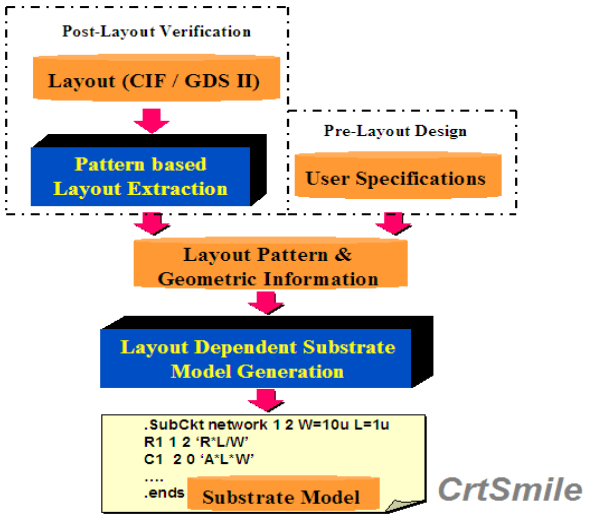

Figure 3. System architecture of *CrtSmile*.

CrtSmile is flexible for incorporating different kinds of substrate networks based on user defined substrate models. Figure 4 shows a substrate network for a four-finger transistor with parallel bulk contacts based on the BSIM4 substrate model. The substrate is a heavily doped one as in Fig. 1 of [12]. In Fig. 4, BI is the intrinsic bulk contact and the back plane is generally connected to the ground. The circled part in Fig. 4 is the BSIM4 substrate model for a single finger. Similar substrate networks can be derived based on other substrate models. In this paper, we will focus on the substrate network model due to [1].

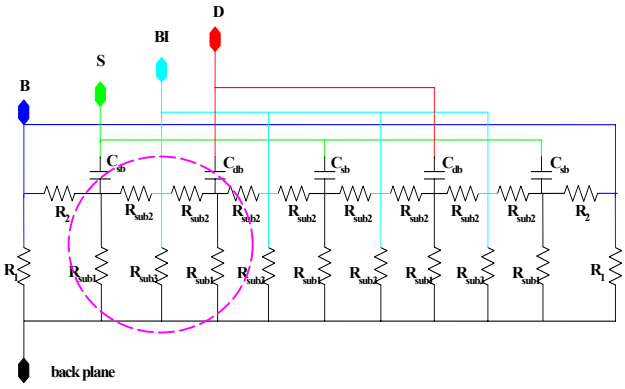

Figure 4. A substrate network based on [2] for a 4-finger transistor.

3. RF transistor layout extraction

Given a layout file in CIF or GDSII formats, the RF transistor layout extraction program is required to recognize different kinds of layout/bulk patterns as well as provide geometric layout information. For a RF transistor layout, there are a few different kinds of layout styles, such as the standard multi-finger layout as in Figs. 2(a) and 2(b), the interleaving layout as in Fig. 2(c), and the dual-gate layout as in Fig. 3 of [6]. Since the substrate resistance is also determined by bulk contact locations, there are also different kinds of bulk contact layout styles that need to be considered. Examples include parallel bulk contacts (Fig. 2(b)), perpendicular bulk contacts (Fig. 2(a)), and guard rings. A traditional layout extraction program will only recognize discrete finger transistors and cannot build the connection between the transistor active regions and bulk contact locations. Therefore, a new pattern based layout extraction program is developed to address these two problems.

The flow of the pattern based RF layout extraction program is shown in Fig. 5.

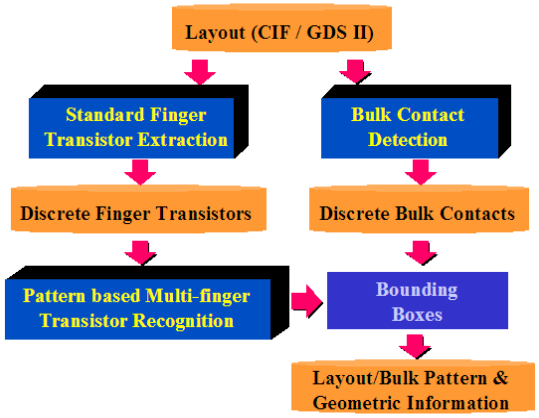

Figure 5. Pattern based RF layout extraction flow.

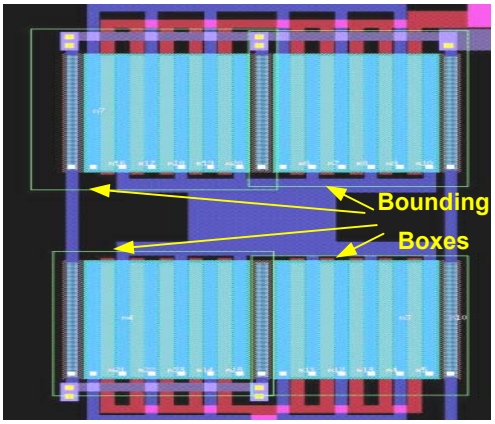

Figure 6. Four multi-finger transistors with four bounding boxes.

First, standard finger transistor extraction and bulk contact detection are performed to have discrete finger transistors and bulk contacts. After that, the pattern based multi-finger transistor recognition module is called to recognize different kinds of user defined multi-finger layout styles based on different electrical connectivity patterns. Then bounding boxes are applied to relate discrete bulk contacts to proper multi-finger transistors and recognize corresponding bulk contact layout styles. Figure 6 shows a bounding box example, in which four bounding boxes are highlighted to extract four multi-finger transistors with parallel bulk contacts. Bounding boxes can be added manually or automatically with the assumption that only bulk contacts close enough to the transistor active regions are related to the corresponding multi-finger transistors. Finally, layout/bulk pattern and geometric layout information is retrieved. The extracted circuit netlist for one of the multi-finger transistors in Fig. 6 is shown below:

```
.subckt T1 nd ng ns gnd Wf=13.00u Lf=0.80u Nf=5 Db=0.60u
m1 nd ng ns nbi NMOS w=Wf l=Lf ad='Wf*1.00u'
+as='Wf*0.50u' pd='2*(Wf+1.00u)' ps='Wf+1.00u'
m2 nd ng ns nbi NMOS w=Wf l=Lf ad='Wf*0.50u'
+as='Wf*0.50u' pd='Wf+1.00u' ps='Wf+1.00u' m='Nf-2'
m3 nd ng ns nbi NMOS w=Wf l=Lf ad='Wf*0.50u'
+as='Wf*1.00u' pd='Wf+1.00u' ps='2*(Wf+1.00u)'
xsub nbi gnd subres_para w='Wf*Nf' l=Lf n=Nf d=Db
.ends
```

where W_f is the finger width, L_f is the channel length, N_f is the number of gate fingers and D_b is the distance of bulk contacts from the transistor active region. The substrate resistance for the parallel bulk contact layout style is represented by a subcircuit

(*subres_para*), which is dependent on geometric layout parameters and will be discussed in Section 4.

4. Scalable layout dependent substrate model

In this section, the substrate resistance (R_{sub}) for multi-finger transistors with parallel bulk contacts is first studied and is further extended to those with perpendicular bulk contacts.

4.1 Substrate model for parallel bulk contacts

A DC extraction of the substrate resistance is used, which is a modification of the method described in [7]. As shown in Fig. 7, p^+ bulk straps replace all gate fingers. A small voltage is applied to the appropriate bulk strap and the other bulk straps are grounded to obtain the substrate resistance of a specified finger. Meanwhile, the bulk contacts and the drain/source contacts are all grounded. The ratio of the applied voltage to the current through the bulk contacts gives the substrate resistance of that finger.

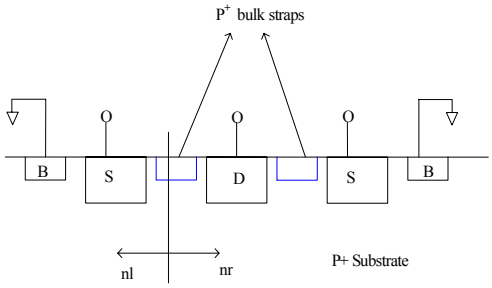

Figure 7. Simulated structure to study the dependence of R_{sub} on multiple gate fingers.

Figure 7 shows the structure that is simulated with the 2D device simulator MEDICI [9] to study the dependence of the substrate resistance on the number of gate fingers. "nl" and "nr" denote the number of gate fingers to the left and right of the gate finger of interest, respectively (i.e., nl=1, nr=2, in Fig. 7).

Figure 8 shows the finger resistance with different nl and nr for a fixed device width of 500 µm. It can be seen that the finger resistance for a fixed nl varies linearly with nr and hence in theory only two points on one straight line are needed to obtain a linear model. It should be noted that only three points on the first two straight lines (A, B, and C as shown in Fig. 8) are required to obtain the finger resistance models for nl=2 and nl=3 since the finger resistance for (nl,nr)=(2,3) is the same as that for (nl,nr)=(3,2). Noting the linear dependence for 2≤nl≤(n-1) and that the finger resistances for (nl,2)=(2,nl) and (nl,3)=(3,nl), the finger resistance for any finger with 2≤nl≤(n-1) can be written as below:

$$\frac{R_{fing}(nl,nr)-R_{fing}(2,nl)}{nr-2}=\frac{R_{fing}(3,nl)-R_{fing}(2,nl)}{3-2} \qquad (1)$$

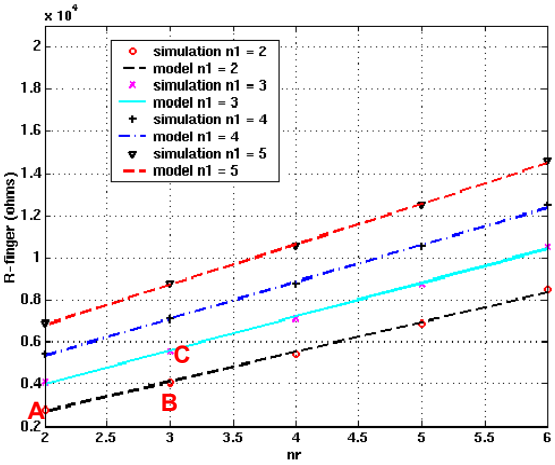

Figure 8. R_{sub} vs. nr for different nl.

Since the finger resistances for the two end fingers dominate the substrate resistance [4], they have been separately modeled using a linear model for accuracy. By obtaining the six finger resistance models for {(nl,nr)}={(1,1), (1,2), (1,3), (2,2), (2,3), (3,3)}, all the finger resistance models can be obtained from Eq. (1). The total substrate resistance R_{sub} for a fixed distance *d* from the bulk contacts to the active region is then calculated using Eq. (2) after all finger resistances have been calculated. In Eq. (2), *W* is the device width and it is seen that R_{sub} for parallel bulk contacts is inversely proportional to *W*.

$$R_{sub}(n,d)=\frac{500\mu}{W}\frac{1}{\sum_{nl=1}^{n}\frac{1}{R_{fing}(nl,nr)}} \qquad (2)$$

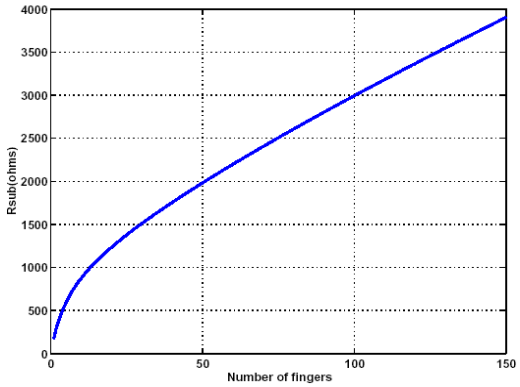

Figure 9. R_{sub} vs. number of fingers for W=500µm.

Figure 9 shows a plot of the R_{sub} variation with the number of gate fingers for a constant device width of 500 µm. It can be observed that R_{sub} increases with *n* and for large *n* has a linear dependence on *n*. This can be explained by observing that for a larger number of gate fingers, the resistance contribution of the interior fingers to the total substrate resistance is insignificant. As the device width is kept constant, the width of each finger scales inversely with the number of fingers. For large *n*, the substrate resistance that is dominated by the end fingers scales inversely with the finger width as *n* increases. Hence, an inverse dependence on the finger width is observed, that translates directly to a linear dependence on *n*.

Figure 10 shows the dependence of R_{sub} on the distance of the bulk contacts from the active region. The simulation is performed for structures with different number of fingers with fixed finger width as the distance *d* is varied from 2 µm to 15 µm. R_{sub} has a linear dependence on *d* for multi-finger transistors with parallel bulk contacts.

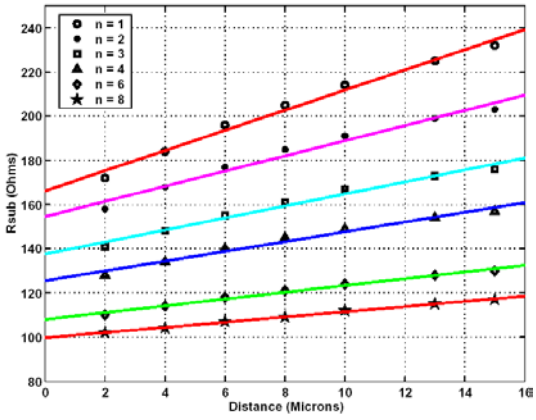

Figure 10. R_{sub} vs. *d* for different number of fingers.

A scalable model for R_{sub} as a function of *n* and *d* can be obtained by combining the previous results of this section as below:

$$R_{sub}(n,d) = \left[\frac{R_{sub}(n,d=d_2) - R_{sub}(n,d=d_1)}{d_2 - d_1}\right] * d + \left[\frac{d_2 * R_{sub}(n,d=d_1) - d_1 * R_{sub}(n,d=d_2)}{d_2 - d_1}\right] \quad (3)$$

Table I shows the values of R_{sub} obtained from device simulations for a MOS transistor with a width of 500 µm and different number of gate fingers for various channel lengths. For the typical channel lengths used in RF applications, R_{sub} has a weak dependence on the channel length. This has also been observed from measurements on a single fingered device [13].

Table I. R_{sub} vs. channel length for different number of fingers.

N / L (µm)	R_{sub} (Ohms)		
	1	4	10
0.6	165	515	950
0.7	163	508	940
0.8	160	502	933
0.9	158	495	925
1.0	155	490	915
2.0	143	465	870

Therefore, Eqs. (1), (2) and (3) describe the scalable substrate model for a multi-finger transistor with parallel bulk contacts as a function of the number of fingers (n), device width (W), and bulk contact locations (d). The dependence on channel length (L) is weak and is not included in the model.

4.2 Substrate model for perpendicular bulk contacts

So far, we have been considering the case where the bulk contacts are placed parallel to the finger direction as shown in Fig. 2(b). However, in certain applications the substrate contacts are placed perpendicular to the finger direction. The structure similar to Fig. 2(a) with two perpendicular bulk contacts is simulated using the 3D device simulator PROPHET [3] for a different number of fingers and the extracted values of the substrate resistance are shown in Table II for a finger width of 10 µm.

It can be seen from Table II that R_{sub} scales inversely with the number of fingers and the error incurred on assuming this scaling is less than 5%. Thus, when the substrate contacts are placed perpendicular to the device active area, R_{sub} is inversely proportional to the number of fingers for a given finger width.

Table II. R_{sub} vs. number of fingers for fixed finger width (10 µm).

n	R_{sub} from PROPHET (Ohms)	R_{sub} scaled from single finger value (Ohms)	% error
1	3400	3400	0
2	1805	1700	5.8
3	1210	1133	6.4
4	893	850	4.8

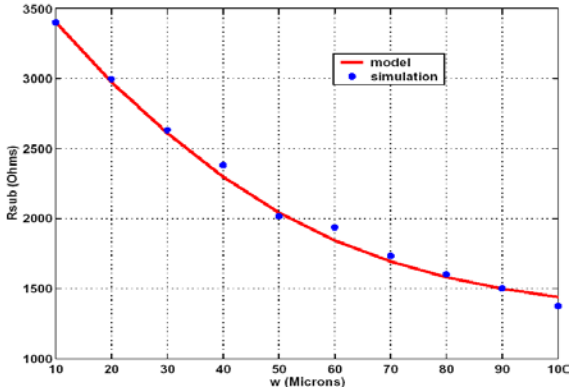

Figure 11. R_{sub} vs. finger width.

Figure 11 shows the R_{sub} variation with the finger width. It can be seen that R_{sub} decreases with an increased finger width and eventually saturates. The equation describing the dependence of R_{sub} on the finger width (W_f) and the finger number (n) is given by:

$$R_{sub} = \frac{1}{n} * \left(\frac{1}{\alpha * W_f^{\,3} - \beta * W_f^{\,2} + \gamma * W_f + \delta} + 1225\right) \quad (4)$$

where the four curve fitting parameters are: α=3.655e-9, β=2.905e-8, γ=0.995e-5, and δ=3.63e-4.

Figure 12 shows a plot of R_{sub} vs. distance d for a single finger transistor with two perpendicular bulk contacts. It can be seen that R_{sub} has a linear dependence on d. Therefore, an equation similar to Eq. (3) can be derived for a scalable layout dependent substrate model for multi-finger transistors with perpendicular bulk contacts.

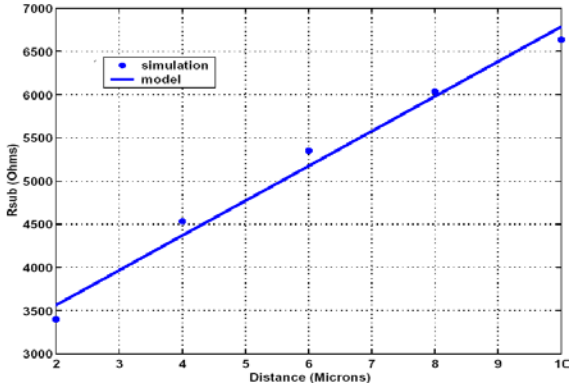

Figure 12. R_{sub} vs. d for perpendicular bulk contacts.

5. Experimental results

5.1 Measurement data of substrate resistance

Various test structures were fabricated in the 0.35 µm TSMC process to study the dependence of the substrate resistance on the layout of the MOS transistors. Figure 13 shows the layout of the test structures excluding the probe pads. The test structures can be divided into six different categories with each category serving a different purpose as shown in Fig. 13. Table IV describes these categories.

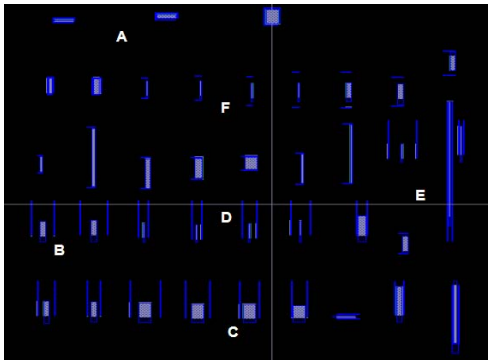

Figure 13. Test structures to study the layout dependent R_{sub}.

Table IV. Description of test structures

Label	Objective	Number of test structures
A	R_{sub} with contacts all around the device	5
B	R_{sub} dependence on distance for 4 fingers	4
C	R_{sub} dependence on distance for 10 fingers	4
D	R_{sub} dependence on distance for 1 finger	4
E	R_{sub} width dependence	7
F	R_{sub} with contacts perpendicular to the device	15

Table V shows the measured values of DC R_{sub} for a single fingered device for three different values of the finger width. The simulation results using the Substrate Coupling Analysis (SCA) tool [14] are also shown. The values of R_{sub} from SCA are in the ballpark of values obtained from measurements. It can be observed that R_{sub} scales inversely with the width of the device.

Table V. Variation of R_{sub} with finger width for a single finger device.

Width (μm)	R_{sub} (Ohms)		R_{sub} scaled from the measured value for W= 25 μm	% error
	SCA	Measurement		
25	165	202	202	0
50	90	106	101	4.7
200	23	28	25.3	9.2

Figure 14 shows a plot of the substrate resistance with the number of fingers for a device width of 200 μm with parallel bulk contacts. It can be seen that R_{sub} has a linear dependence on n for n > 2 and the linear model matches closely with the measured data. This justifies the simulated results observed in Fig. 9 of Section 4. Figure 15 shows the plot of R_{sub} with distance of the bulk contacts for devices with 1, 4 and 10 fingers, respectively. The finger width is 25 μm. Consistent with simulations in Fig. 10 of Section 4, the measured values of R_{sub} show a linear dependence on *d*.

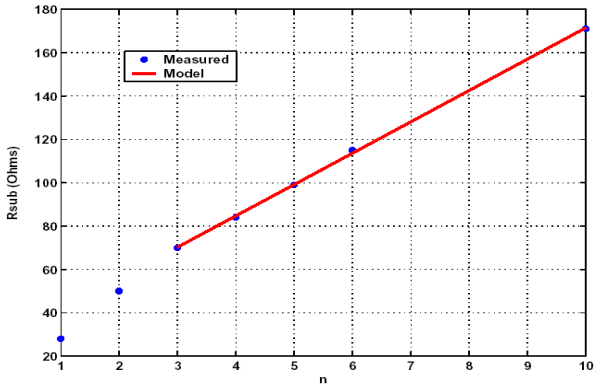

Figure 14. R_{sub} vs. number of fingers for W=200 μm.

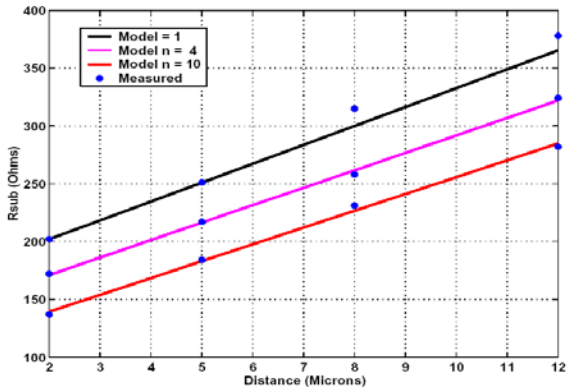

Figure 15. R_{sub} vs. *d* for a finger width of 25 μm.

5.2 Low noise amplifier

Figure 16 shows a 2.4 GHz common source low noise amplifier (LNA), in which the substrate resistances for multi-finger transistors (M1 and M2) are included to account for the silicon substrate. As discussed in Section 4, the value of the substrate resistance is dependent on the layout/bulk patterns and the geometric layout information. For this example, a standard multi-finger layout style with parallel bulk contacts is used. Both M1 and M2 are realized with 1-finger and 4-finger layout styles to show how the layout and, hence, R_{sub} affect the LNA performance. The substrate resistance model is the same as that discussed in Section 4.1. According to Fig. 9, for a transistor with a device size of 300μm, R_{sub}=267 Ω for a 1-finger layout style (R_{sub}= 500/300*160≈267 Ω), and R_{sub}=850 Ω for a 4-finger layout style (R_{sub}=500/300*510=850 Ω).

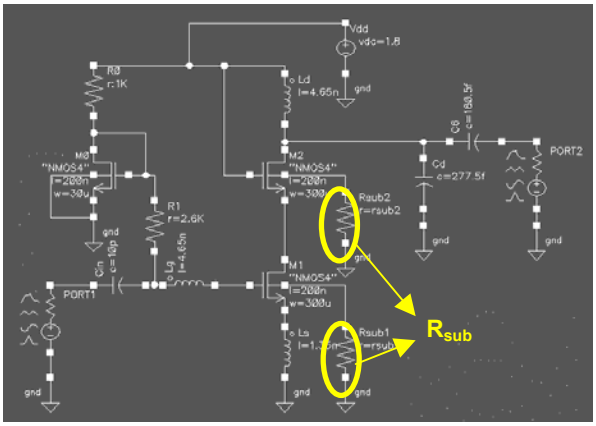

Figure 16. A low noise amplifier with substrate resistance.

Figure 17 and Figure 18 show the gain (S21) and noise figure (NF) of the LNA for both 1-finger and 4-finger layout styles. The LNA is first designed without considering the substrate resistance. The performance is then compared to an LNA in which the substrate resistance is included in the simulations. It can be seen that the substrate resistance has a significant influence on the LNA performance. Due to the substrate resistance, the gain is decreased and the noise figure is increased for these two layout styles. Since the substrate resistance is related to layout, a layout dependent substrate model is necessary for RF circuit design to properly account for the substrate effects. Although the substrate resistance is larger for a 4-finger layout style, the LNA performance degeneration is still less since parasitic capacitors (C_{db} and C_{sb}) for multi-finger transistors are decreased. On the other hand, it is obvious that the smaller the substrate resistance is the better is the agreement with a design without the substrate resistance.

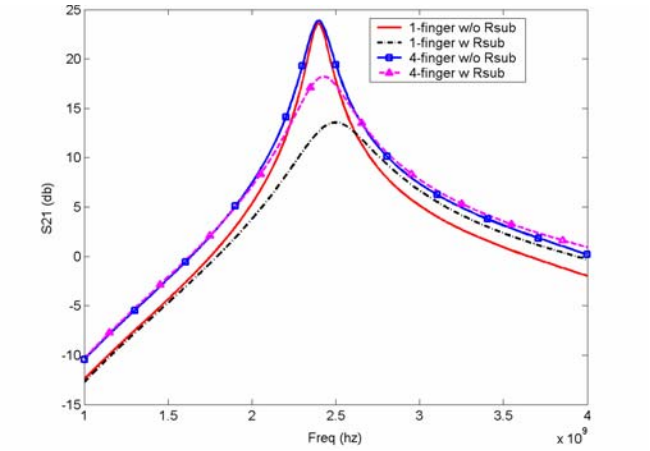

Figure 17. S21 for LNA with transistors in 1-finger and 4-finger layout styles.

For a standard multi-finger layout with parallel bulk contacts, the number of fingers has to be small to achieve a small substrate resistance as shown in Fig. 9. This will, unfortunately, introduce larger parasitic capacitance effects. Therefore, there exists a design tradeoff between the substrate resistance and parasitic capacitors. By using layout dependent substrate models, a RF circuit can be optimized for a proper layout/bulk pattern. In this manner, a good balance between the RF performance, parasitic effects, layout area, layout variation due to process variation, etc. can be achieved.

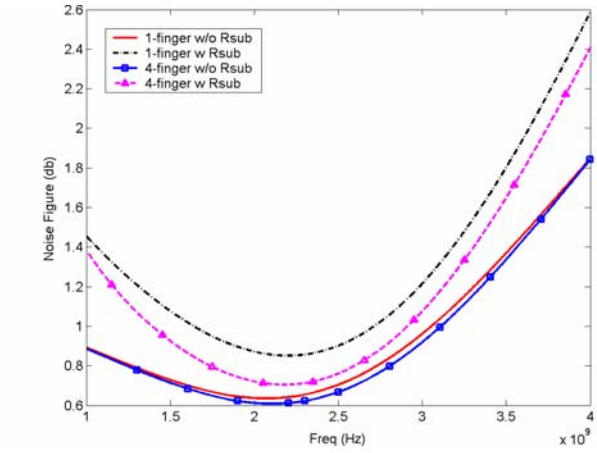

Figure 18. Noise figure for LNA with transistors in 1-finger and 4-finger layout styles.

6. Conclusions

This paper presents a layout dependent substrate model generation system *CrtSmile*. *CrtSmile* reads RF transistor layout files as the input and applies a pattern based layout extraction program to extract different kinds of layout/bulk patterns and geometric layout information. A scalable substrate model for multi-finger transistors is developed, which is dependent on the RF transistor layout/bulk patterns and geometric layout information, such as the number of fingers, finger width, channel length, and bulk contact locations. This model gives good agreement with the measured data for a 0.35µm CMOS process. A low noise amplifier example is further studied with the new layout dependent substrate model and shows the importance of CMOS RF transistor layout on substrate resistance modeling.

7. Acknowledgements

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8. References

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