Behavioral group meeting held on 25 October 2002

Present

Bo Hu, Bo Wan, Yong Wang, Lili Zhou, Gus Mak, Chris Baker, Kishore Tanikella, Guoyong Shi, Pavel Nikitin

Highlights

- Bo Hu and Bo Wan gave a short presentation on compiler limitations
- Discussion followed
    - The compiler is targeted for fast implementation of new device models into a circuit simulator
    - Circuit- and block- level behavioral modeling or digital simulations are not supported and are not a focus of efforts

Progress/current work

- Learning/reading papers on VHDL-AMS (Chris, Gus, Kishore, Pavel)
- Reading on behavioral modeling of D/A converters (Kishore)
- MOS transistor modeling with Verilog/VHDL-AMS (Lili, Chris, Gus)
- Boeing designs clarification (Yong)
- Compiler work (Bo Hu, Bo Wan)

Next week plan

- Instructions on running the compiler will be posted
- Run test examples using the compiler, compare the results with Cadence, where possible
- Understand features/limitations of other commercially available VHDL-AMS simulators