DARPA CAD WorkShop

Next Generation CAD Tools For Gigascale Integrated Mixed Technology System-On-A-Chip Workshop
CD-ROM

Arlington, Virginia
May 5, 2000

Anantha Krishnan
DARPA Program Mananger

Table of Contents

NEXT GENERATION CAD TOOLS FOR
GIGASCALE INTEGRATED MIXED TECHNOLOGY
SYSTEM-ON-A-CHIP WORKSHOP

DARPA –MTO
May 5, 2000

Welcome/Introduction

Anantha Krishnan	DARPA/MTO

Device Technology

Christie Marrian	DARPA/MTO
Gerhard Klimeck	NASA/JPL
Robert Dutton	Stanford
James Ellenbogen	MITRE

Device Integration

Dan Radack	DARPA/MTO
Don MacMillen	Synopsys
Wojciech Maly	Carnegie Mellon University
Don Cottrell	Si2
Steve Levittan	University of Pittsburgh

System-on-a-Chip (SoC) Technology

Jim Murphy/Edgar Martinez	DARPA/MTO
Bob Hillman	AFRL/Rome
Bob Broderson	University of California, Berkeley
Mehdi Kazemi-Nia	Cognet Microsystems
Jacob White	MIT
Zachary Lemnios	MIT/LL

Presentations by Session Leaders (Break-out Sessions)

Device Technology

Device Integration

System-on-a-Chip Technology

DARPA CAD Workshop

Final Attendees List
Arlington, VA
May 5, 2000

Lawrence Arledge
SRC
CADTS
P.O. Box 12053
Research Triangle Park, NC 27712
Work #: 919-941-9400
Fax #: 919-941-9450
Email: Arledge@SRC.org

Robert Brodersen
University of California at Berkeley
Department of EECS
Cory Hall, Room 402
Berkeley, CA 94720-1774
Work #: 510-642-1779
Fax #: 510-883-2070
Email: rb@eecs.berkeley.edu

Felix Buot
Naval Research Laboratory
Electrical Science and Technology Division
4555 Overlook Avenue SW
Washington, DC 20375
Work #: 202-767-2644
Fax #: 202-767-0546
Email: buot@estd.nrl.navy.mil

Frank Crowne
Army Research Laboratory
RF Electronics
2800 Powder Mill Road
Adelphi, MD 20783
Work #: 301-394-5759
Fax #: 301-394-2525
Email: fcrowne@arl.mil

Sara Dao
System Planning Corporation
1429 North Quincy Street
Arlington, VA 22207
Work #: 703-351-8610
Fax #: 703-351-8862
Email: sdao@sysplan.com

Robert Dutton
Stanford University
Electrical Engineering
CISX 333
Stanford, CA 94305-4075
Work #: 650-723-4138
Fax #: 650-725-7731
Email: dutton@ee.stanford.edu

DARPA CAD Workshop
Final Attendees List
Arlington, VA
May 5, 2000

James Ellenbogen
The MITRE Corporation
Nanosystems Group
1820 Dolley Madison Boulevard
McLean, VA 22102
Work #: 703-883-5930
Fax #: 703-883-5963
Email: ellenbgn@mitre.org

Gary Fedder
Carnegie Mellon University
Electrical and Computer Engineering
5000 Forbes Avenue
Pittsburgh, PA 15213-3890
Work #: 412-268-8443
Fax #: 412-268-3890
Email: fedder@ece.cmu.edu

David Ferry
Arizona State University
Department of Electrical Engineering
Box 875706
Tempe, AZ 85287-5706
Work #: 480-965-2570
Fax #: 480-965-8058
Email: ferry@asu.edu

Harold Grubin
Scientific Research Associates, Inc.
P.O. Box 1058
Glastonbury, CT 06033
Work #: 860-659-0333
Fax #: 860-633-0676
Email: hal@srassoc.com

Claire Heller
System Planning Corporation
1429 North Quincy Street
Arlington, VA 22207
Work #: 703-351-8619
Fax #: 703-351-8862
Email: cheller@sysplan.com

Carol Higgins
System Planning Corporation
1429 North Quincy Street
Arlington, VA 22207
Work #: 703-351-8617
Fax #: 703-351-8662
Email: chiggins@sysplan.com

DARPA CAD Workshop

Final Attendees List
Arlington, VA
May 5, 2000

Jim Hilger
STA
4001 Fairfax Drive
Arlington, VA 22203
Work #: 703-522-5123
Fax #: 703-522-0367
Email: jhilger@stassociates.com

Robert Hillman
Air Force Research Laboratory
IFTE
26 Electronic Parkway
Rome, NY 13441-4514
Work #: 315-330-4961
Fax #: 315-330-2953
Email: hillmanr@rl.af.mil

Mehdi Kazemi-Nia
CogNet MicroSystems
11500 West Olympic Blvd.
Suite #611
Los Angeles, CA 90064
Work #: 310-231 8242
Fax #: 310- 231 0702
Email: mkazeminia@mail.cognetmicro.com

Gerhard Klimeck
Jet Propulsion Laboratory
California Institute of Technology
Techical Staff and Application Group
4800 Oak Group Drive, MS 168-522
Pasenda, CA 91125
Work #: 818-354-2182
Fax #: 818-393-3155
Email: gekco@polo.jpl.nasa.gov

Anantha Krishnan
Defense Advanced Research Projects Agency
Microsystems Technology Office
3701 North Fairfax Drive
Arlington, VA 22203-1714
Work #: 703-696-4470
Fax #: 703-696-2206
Email: akrishnan@darpa.mil

Robert Leheny
Defense Advanced Research Projects Agency
Microsystems Technology Office
3701 North Fairfax Drive
Arlington, VA 22203-1714
Work #: 703-696-0048
Fax #: 703-696-2206
Email: rleheny@darpa.mil

DARPA CAD Workshop

Final Attendees List
Arlington, VA
May 5, 2000

Zachary Lemnios
MIT Lincoln Laboratory
Solid State Division
244 Wood Street
Lexington, MA 02420-9108
Work #: 781-981-7802
Fax #: 781-981-5024
Email: zlemnios@ll.mit.edu

Steven Levitan
University of Pittsburgh
Department of Electrical Engineering
348 Benedum Hall
Pittsburgh, PA 15261
Work #: 412-648-9663
Fax #: 412-624-8003
Email: steve@ee.pitt.edu

Per Ljung
Coyote Systems
2740 Van Ness Avenue #210
San Francisco, CA 94109
Work #: 415-346-4223, Ext. 12
Fax #: 415-346-6282
Email: pbljung@coyotesystems.com

Don MacMillen
Synpsys, Inc
Advanced Technology Group (ATG)
700 East Middlefield Rd. C-22
Mountain View, CA 94043
Work #: 650-584-1985
Fax #: not given
Email: mac@synopsys.com

Mary Ann Maher
MEMSCAP Inc.
4601 Six Forks Road
Suite 500
Raleigh, NC 27609
Work #: 919-510-8138
Fax #: 919-571-8805
Email: mary-ann.maher@memscap.com

Sharad Malik
Princeton University
Electrical Engineering
Princeton, NJ 08540
Work #: 609-258-4625
Fax #: not given
Email: malik@princeton.edu

DARPA CAD Workshop
Final Attendees List
Arlington, VA
May 5, 2000

Wojciech Maly
Carnegie Mellon University
Electrical and Computer Engineering
5000 Forbes Avenue
Pittsburgh, PA 15213
Work #: 412-268-6637
Fax #: not given
Email: maly@ece.cmu.edu

Christie Marrian
Defense Advanced Research Projects Agency
Microsystems Technology Office
3701 North Fairfax Drive
Arlington, VA 22203-1714
Work #: 703-696-2213
Fax #: 703-696-2206
Email: cmarrian@darpa.mil

Edgar Martinez
Defense Advanced Research Projects Agency
Microsystems Technology Office
3701 North Fairfax Drive
Arlington, VA 22203-1714
Work #: 703-696-7436
Fax #: 703-696-2206
Email: emartinez@darpa.mil

Meyya Meyyappan
National Aeronautics & Space Administration
Ames Research Center
Mail Stop 229-3
Moffett Field, CA 94035-1000
Work #: 650-604-2616
Fax #: 650-604-5244
Email: meyya@orbit.arc.nasa.gov

James Murphy
Defense Advanced Research Projects Agency
Microsystems Technology Office
3701 North Fairfax Drive
Arlington, VA 22203-1714
Work #: 703-696-2250
Fax #: 703-696-2206
Email: jmurphy@darpa.mil

Marty Peckerar
Naval Research Laboratory
Electronic Science and Technology
4555 Overlook Avenue, SW
Washington, DC 20375
Work #: 202-767-3096
Fax #: not given
Email: peckerar@estd.nrl.navy.mil

DARPA CAD Workshop

Final Attendees List
Arlington, VA
May 5, 2000

Joel Phillips
Cadence Design Systems, Inc.
555 River Oaks Pkwy.
Bldg. 3, M/S-3B1
San Jose, CA 95134
Work #: 408-944-7983
Fax #: not given
Email: jrp@cadence.com

William Phillips
Defense Advanced Research Projects Agency
3701 N. Fairfax Drive
Arlington, VA 22203
Work #: 703-696-4468
Fax #: not given
Email: wphillips@darpa.mil

Andrzej Przekwas
CFD Research Corporation
Cummings Research Park
215 Wynn Drive
Huntsville, AL 35805
Work #: 256-726-4815
Fax #: 256-726-4806
Email: ajp@cfdrc.com

Daniel Radack
Defense Advanced Research Projects Agency
Microsystems Technology Office
3701 North Fairfax Drive
Arlington, VA 22203-1714
Work #: 703-696-2216
Fax #: 703-696-2206
Email: dradack@darpa.mil

Umberto Ravaioli
University of Illinois at Urbana - Champaign
Beckman Institute and Department of
Electrical and Computer Engineering
3255 Beckman, 405 N. Mathews
Urbana, IL 61801
Work #: 217-244-5765
Fax #: 217-244-4333
Email: ravaioli@uiuc.edu

Nanette Rushing
System Planning Corporation
1429 North Quincy Street
Arlington, VA 22207
Work #: 703-351-8831
Fax #: 703-351-8862
Email: nrushing@sysplan.com

DARPA CAD Workshop

Final Attendees List

Arlington, VA

May 5, 2000

Michael Shur
Rensselaer Polytechnic Institute
CSE and CIEEM
CII-9017, 110th 8th Street
Troy, NY 12180-3590
Work #: 518-276-2201
Fax #: 518-276-2990
Email: shurm@rpt.edu

Clare Thiem
Air Force Research Laboratory
IFTC
26 Electronic Parkway
Rome, NY 13441-4514
Work #: 315-330-4893
Fax #: 315-330-2953
Email: thiemc@rl.af.mil

Elias Towe
Defense Advanced Research Projects Agency
Microsystems Technology Office
3701 North Fairfax Drive
Arlington, VA 22203-1714
Work #: 703-696-0045
Fax #: 703-696-2206
Email: etowe@darpa.mil

Jacob White
Massachusetts Institute of Technology
50 Vassar Street, Room 36-817
Cambridge, MA 02139
Work #: 617-253-2543
Fax #: 617-258-5846
Email: white@rle-vlsi.mit.edu

Jason Woo
University of California, Los Angeles
Electrical Engineering
56-147K Eng IV
Los Angeles, CA 90095
Work #: 310-206-3279
Fax #: 310-206-8495
Email: woo@icsl.ucla.edu

Peter Wyatt
MIT Lincoln Laboratory
244 Wood Street
Lexington, MA 02420-9108
Work #: 781-981-7882
Fax #: not given
Email: wyatt@ll.mit.edu

DARPA CAD Workshop

Final Attendees List
Arlington, VA
May 5, 2000

Chih-Kong Ken Yang
University of Calfornia, Los Angeles
56-147A Engineering IV, Box 951594
Los Angeles, CA 90095
Work #: 310-206-3665
Fax #: 310-206-8495
Email: yang@ee.ucla.edu

AGENDA

NEXT GENERATION CAD TOOLS FOR GIGASCALE INTEGRATED MIXED TECHNOLOGY SYSTEM-ON-A-CHIP WORKSHOP

8:00	Anantha Krishnan	DARPA/MTO
8:10	Robert Leheny (Director)	DARPA/MTO
8:20	Christie Marrian	DARPA/MTO
8:35	Gerhard Klimeck	NASA/JPL
8:55	Robert Dutton	Stanford
9:15	James Ellenbogen	MITRE
9:50	Dan Radack	DARPA/MTO
10:05	Don MacMillen	Synopsys
10:25	Wojciech Maly	Carnegie Mellon University
10:45	Don Cottrell	Si2
11:05	Steve Levittan	University of Pittsburgh

12:00	Jim Murphy/Edgar Martinez	DARPA/MTO
12:20	Bob Hillman	AFRL/Rome
12:40	Bob Broderson	University of California, Berkeley
1:00	Mehdi Kazemi-Nia	Cognet Microsystems
1:20	Jacob White	MIT
	Zachary Lemnios	MIT/LL

Device Technology

Device Integration

System-on-a-Chip (SoC) Technology

Presentations by Session Leaders

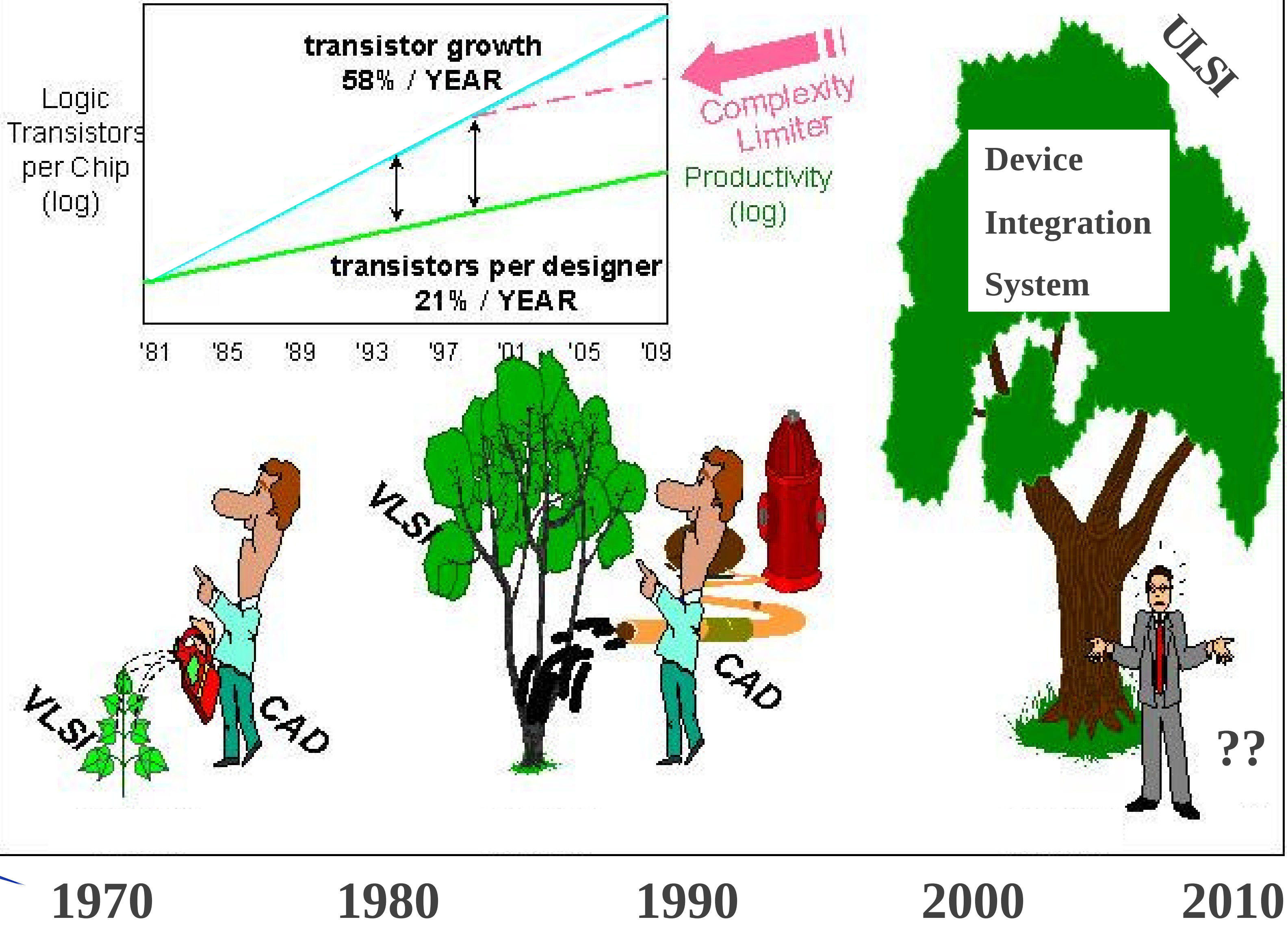
4:15-4:35	Device Technology	
4:35-4:55	Device Integration	
4:55-5:15	System-on-a-Chip Technology	
5:15	Anantha Krishnan	DARPA/MTO

Workshop
on
Next Generation CAD Tools for Gigascale Integrated Mixed Technology System-on-a-Chip

Anantha Krishnan
DARPA/MTO

May 5, 2000
Arlington, VA

Evolution of VLSI and CAD



Design Challenges

Nanodevices (Very Small)

- Quantum Tunneling Effects
- Thermal Noise, Impurities, …
- Quantum Devices, Molecular Electronics, …

Integration (Very Many)

- Deep Sub-Micron Effects
  - Interconnect Latency, Cross Talk, Electromigration, …
  - Power Dissipation/Management
- Novel Integration Ideas, Design Challenges, …

System-on-a-Chip (Very Different)

- Mixed Signal (Digital and Analog)
- Mixed Technology (Electronics, MEMS, Microfluidics, …)
- Hardware and Software

Questions

- What are the projected technology directions and how is it going to affect our ability to design devices/systems in this technology area?
- How will design be done 10 years from now? What are the most critical design challenges and roadblocks that need to be overcome?
- What is the current state of tools in this area? What changes are necessary to accommodate the future challenges? Are these changes incremental and evolutionary? Or do we need to completely change the way things are done now (revolutionary)?
- How do we prioritize the developments? What are the key technical barriers that DARPA needs to address so that we reduce the activation energy for industry to pitch in and invest for continued development?
- What benefits will the military get from this investment? Or to put it in another way, why does DARPA need to invest in this area given that the industry is mature enough and has the necessary resources to address these problems?

Breakout Sessions

Session Leaders :

Device Technology – Meyya Meyyappan

Device Integration - Robert Dutton

System-on-a-Chip - Gary Fedder

DARPA CAD Workshop

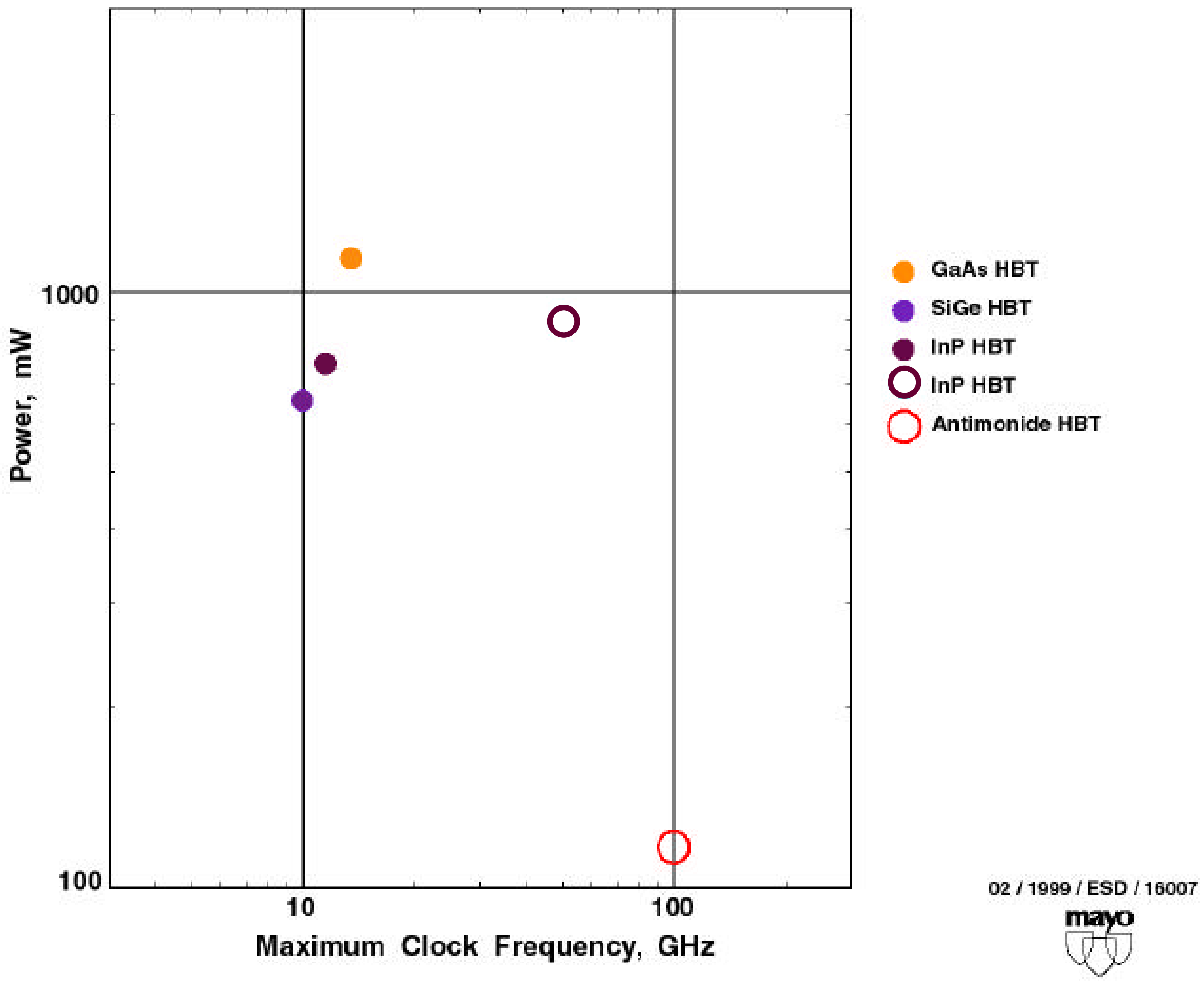
- **Device** (and Circuit) Challenges
  - Nanoelectronics
    - *Ensemble rather than individual devices*
  - Very High Frequencies ~100 GHz
    - *The device – circuit ‘gap’*
  - Defect and Fault Tolerance
    - *Molecular Electronics*
    - *Single Electronics*
  - Non-Electronic Device Gating
    - *Sensors*
    - *Molecular diodes*

Christie Marrian, DARPA/MTO

May 5th, 2000

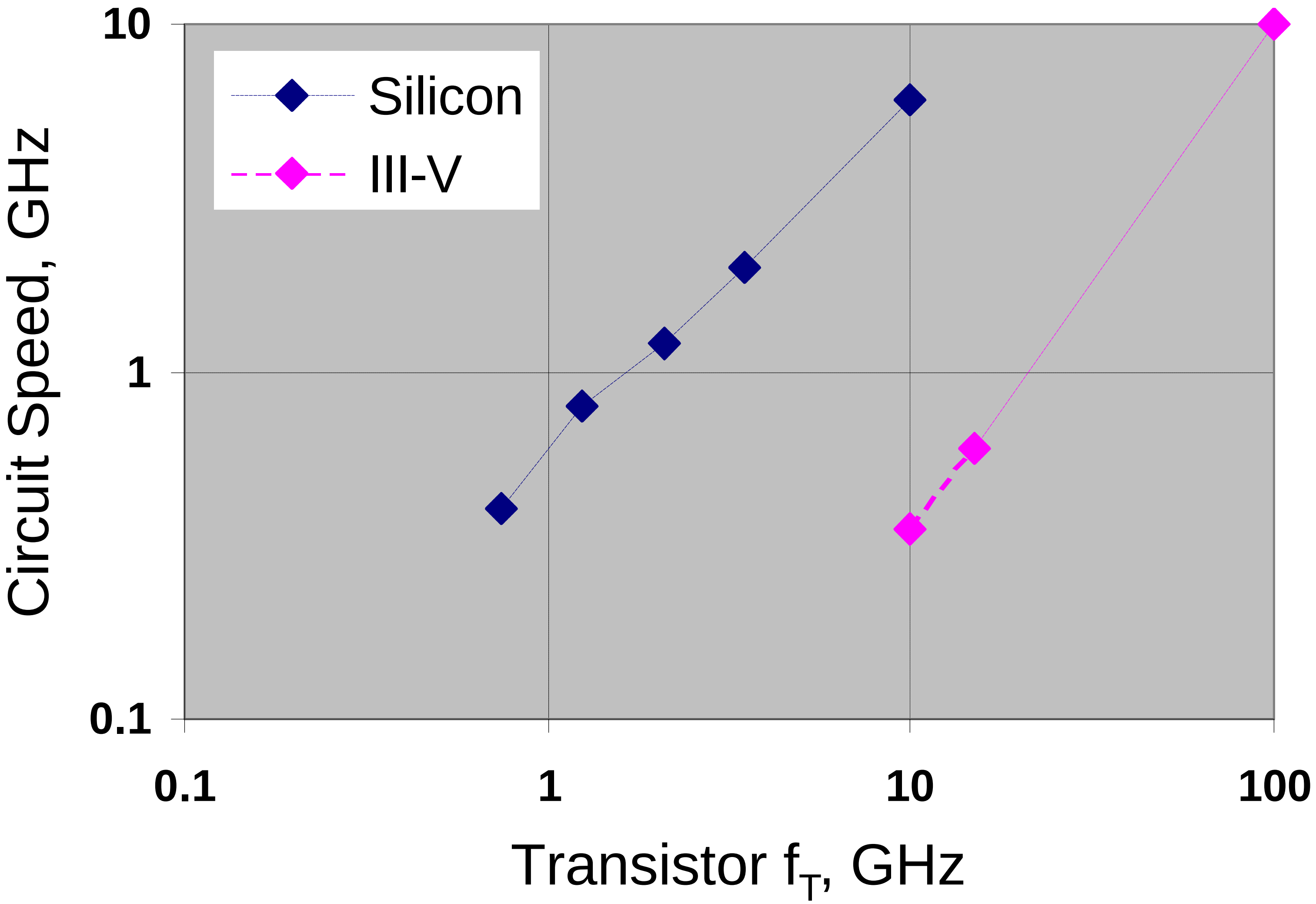
Electronics Integration

Circuit Design: Improvement with Antimonide HBT



2:1 Mux/Demux HSPICE CML logic circuit simulation

Circuit Speed vs. Transistor Speed



Architecture and Defects

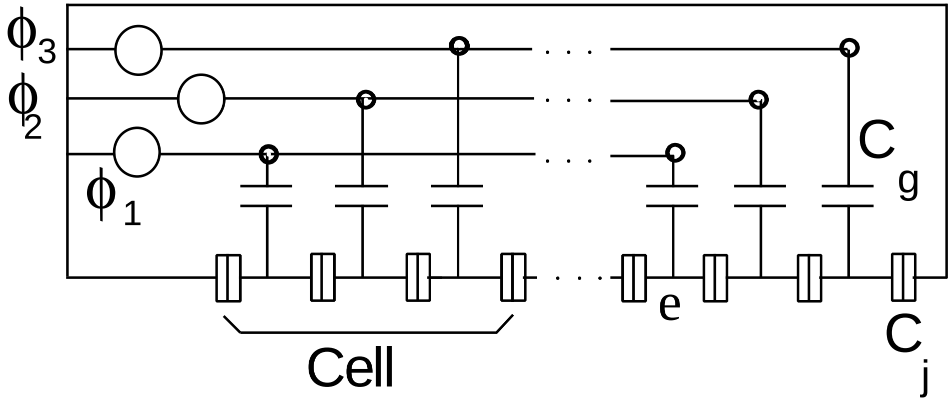
When even a single defect could be a real problem

When defects won't necessarily be a disaster

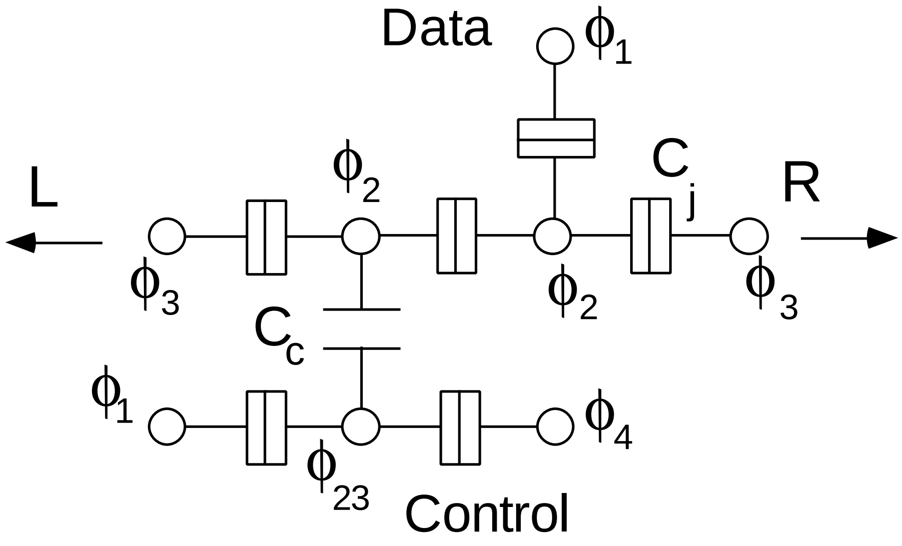
- Defect tolerance
- Logic

SEDC Building Blocks

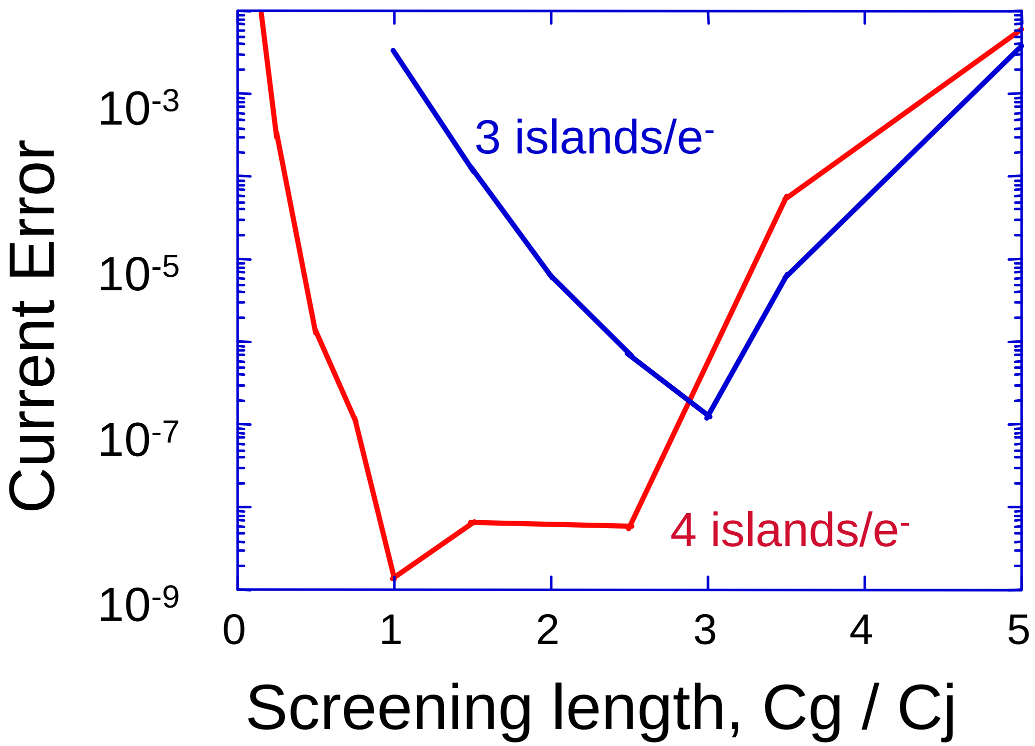
Single-Electron
Shift Register



Single-Electron
Switch



Robustness in Single Electronics



- SE Shift Register
  with 12 islands
- Single Occupancy
- Timed Output
- T = 0

- Optimum screening length is about one island
  - <1: Remote biasing effects cause unwanted transitions
  - >1: Small inter-island coupling leads to frequency errors
- 4-islands/electron circuit reduces co-tunneling.

Mario Ancona, NRL

Defects - How To Deal With Them Using Hardware

Lots of Wires for Communication Bandwidth

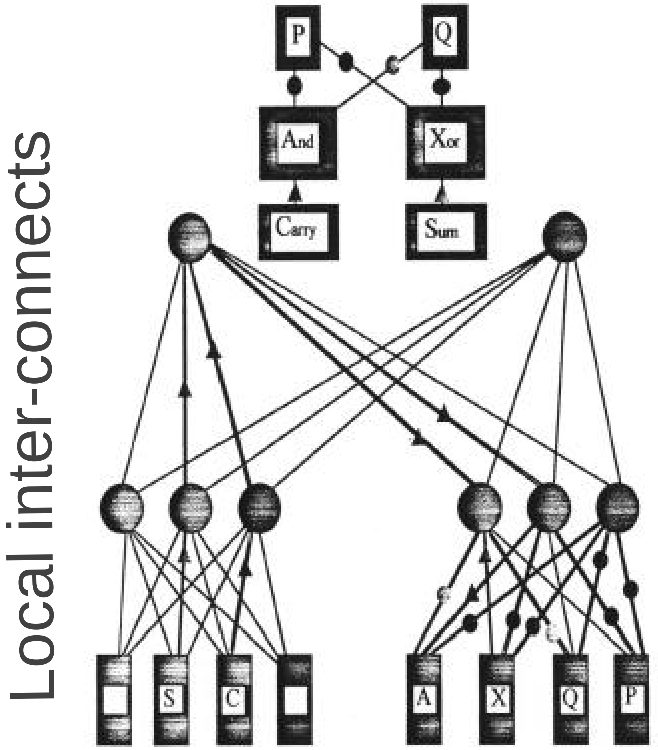
e.g., Fat Tree Architecture

Issues:

- Resistive losses with so many wires
- Testing time to route around defects
- Increased complexity

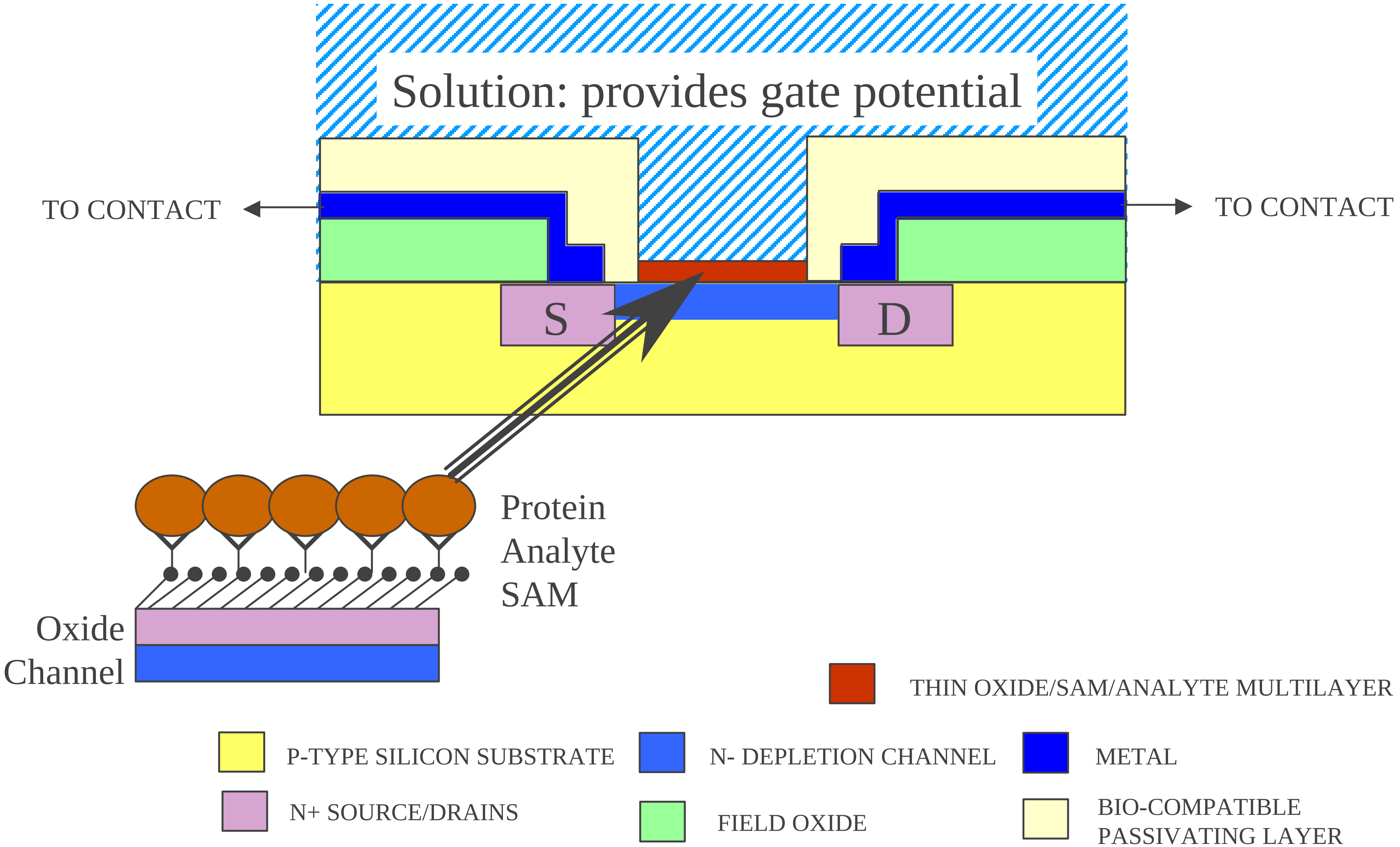
Approach:

- More efficient defect tolerant schemes



Heath, UCLA, Keukes, Snider & Williams, HP Labs, Science, 280 (1998)

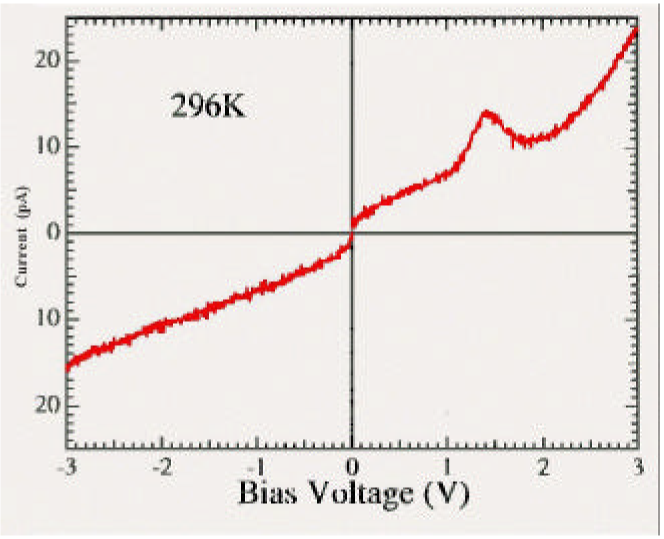
NRL BIOFET

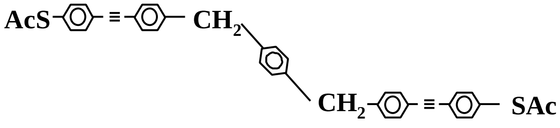

Solution: provides gate potential
TO CONTACT
TO CONTACT
S
D
Protein
Analyte
SAM
Oxide
Channel
THIN OXIDE/SAM/ANALYTE MULTILAYER
P-TYPE SILICON SUBSTRATE
N- DEPLETION CHANNEL
METAL
N+ SOURCE/DRAINS
FIELD OXIDE
BIO-COMPATIBLE
PASSIVATING LAYER

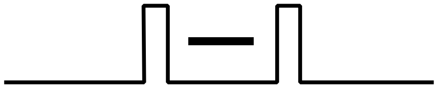
Electrical Properties of Molecular Diodes

- Self-assembling end groups behave as Schottky barriers
- Two non-linear diode mechanisms identified

Resonant Tunneling

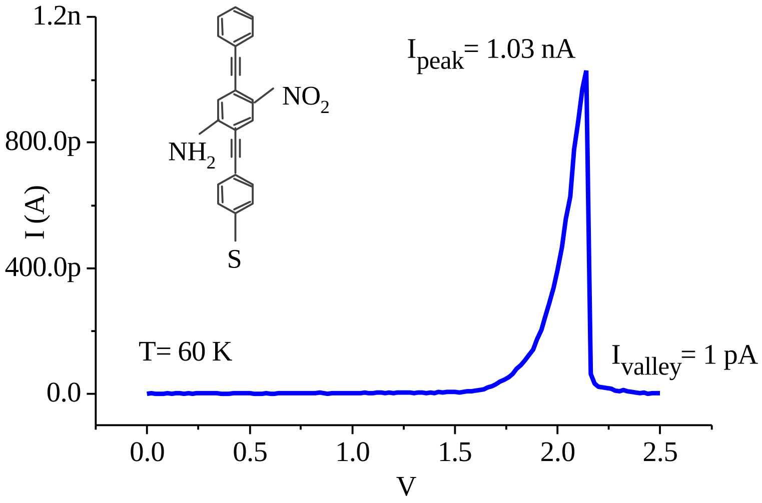


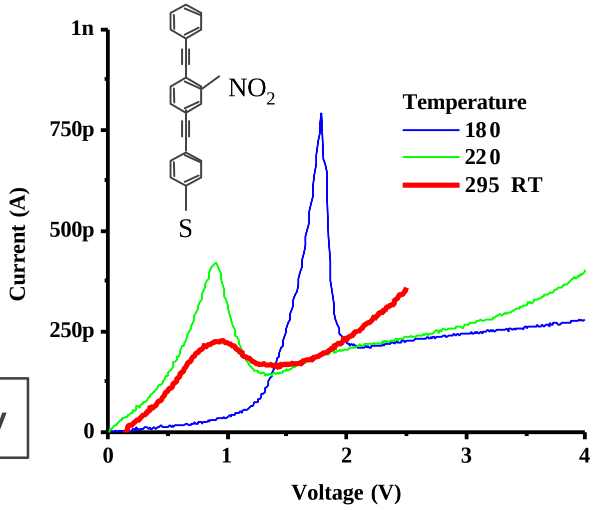




Oxidation/Reduction

PVR = 1030:1
J = 53 A/cm^2
NDR = -380 mW-cm^2





Control of electronic properties by chemistry

Yale University, Rice University

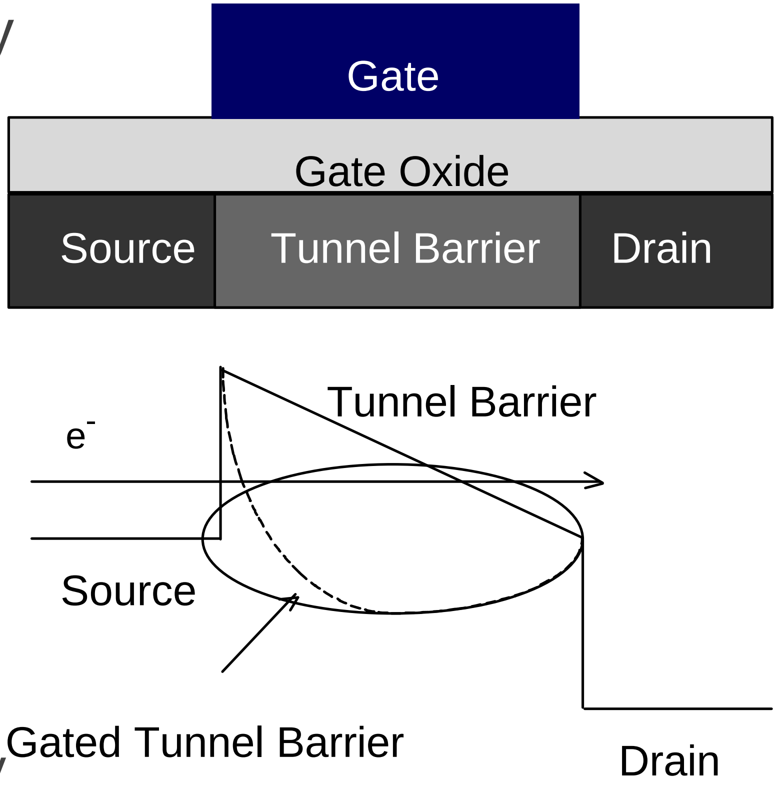
DARPA CAD Workshop

- Device and Circuit Challenges
  - Nanoelectronics
  - Very High Frequencies ~100 GHz
  - Defect and Fault Tolerance
  - Non-Electronic Device Gating

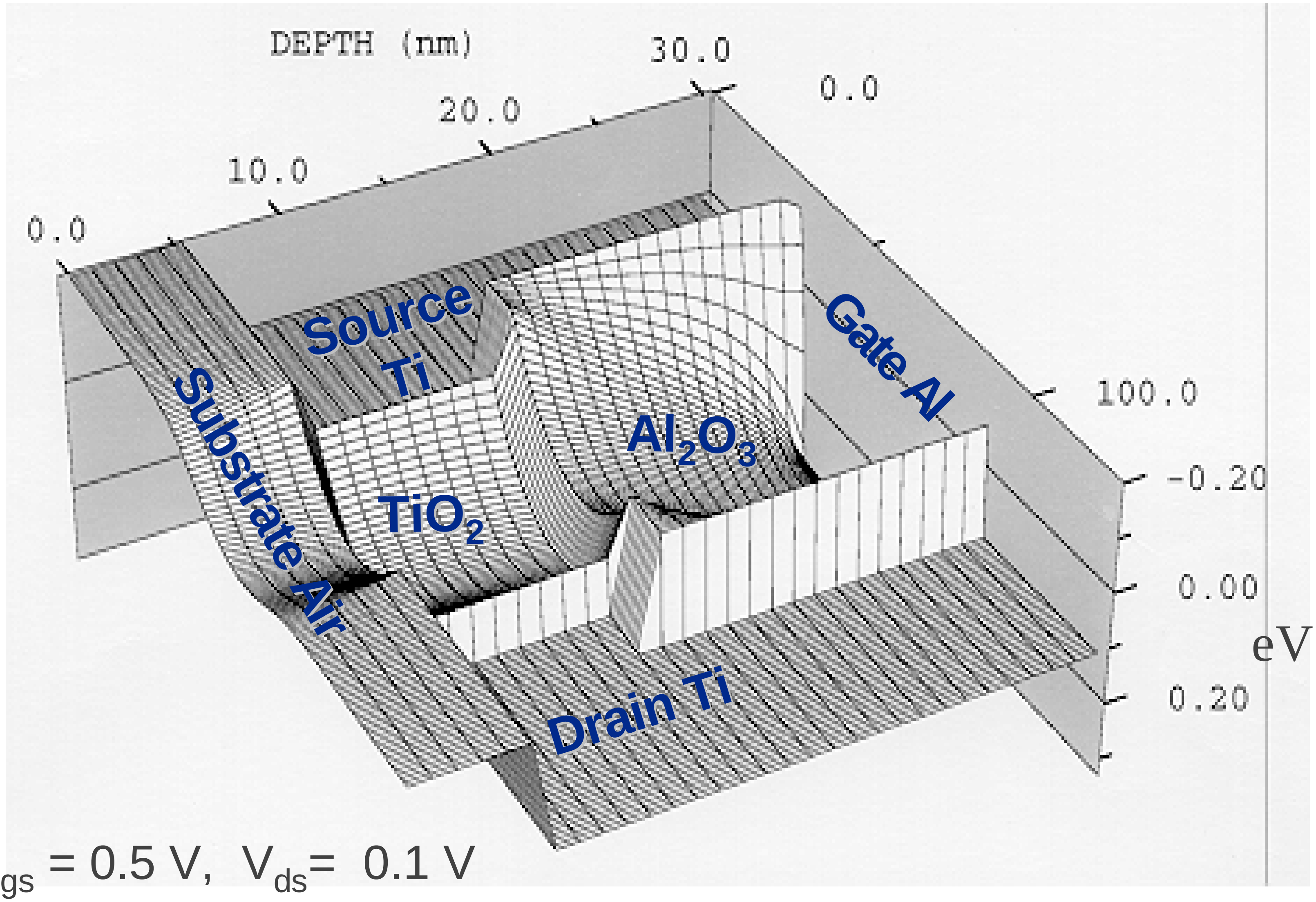
Need to consider the device physics, (chemistry) in the context of the circuit/system

Gate-Modulated Tunneling Transistor

- Gate field alters *shape* of tunnel barrier potential
- Current depends exponentially on effective tunnel barrier width
- Gate bias modulates width of tunnel barrier to cause huge change in tunnel current
  - High transconductance
- Key challenge: fabrication of high-quality lateral tunnel junctions
  - NRL approach: metal/metal oxide junctions fabricated by AFM induced anodic oxidation



Calculated Equipotential Surfaces for Ti/TiO_2 Device



V_{gs} = 0.5 V, V_{ds} = 0.1 V

Defects Are There: How To Deal With Them Using Algorithms

Old Way: Precision Design and Build

Design - Build - Compile - Run

New Way: Directed Design and Self-Assembly

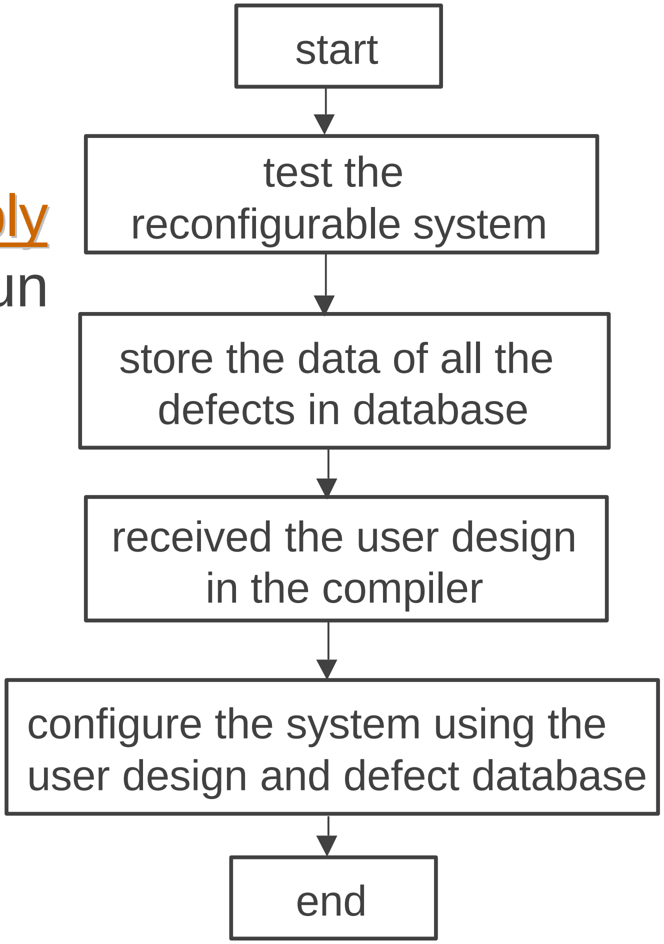
Build - Measure - Reconfigure - Compile - Run

Issues:

- Time needed to route around defects
- Machine test itself
- Reproducibility (intra and inter)

Approach:

- Modular search test/algorithms



start

test the reconfigurable system

store the data of all the defects in database

received the user design in the compiler

configure the system using the user design and defect database

end

Culbertson & Kuekes, US Patent #5,790,771 (1998)

Heath, Keukes, Snider & Williams, Science, 280 (1998)

Chemically Optimize Electronic Functionality

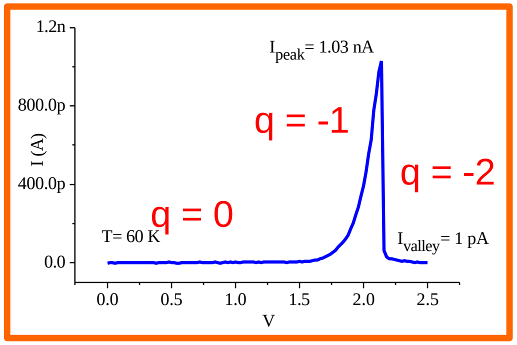
Issues:

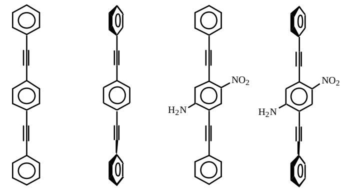
- high temperature operation
- storage time
- “on” resistance
- on:off ratios

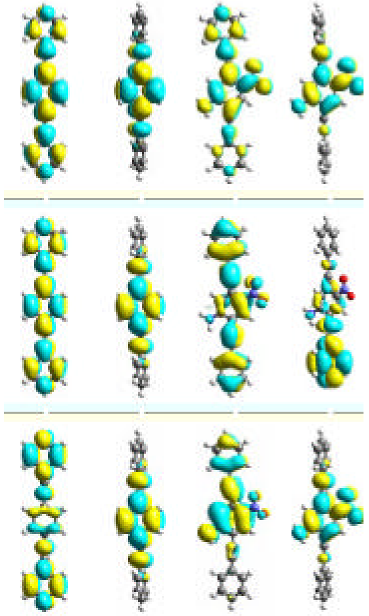
Approach:

- chemical optimization
- modeling

Negative differential resistance







0

-1

-2

Yale Univ., Rice Univ., Univ. South Carolina

Single Electronics: Issues & Plans

- Identification of Coulomb blockade mechanism in AlSb/InAs material system
  - Virtual dot or defect
- Investigate transport through asymmetric junctions
- Control screening length for logic operations

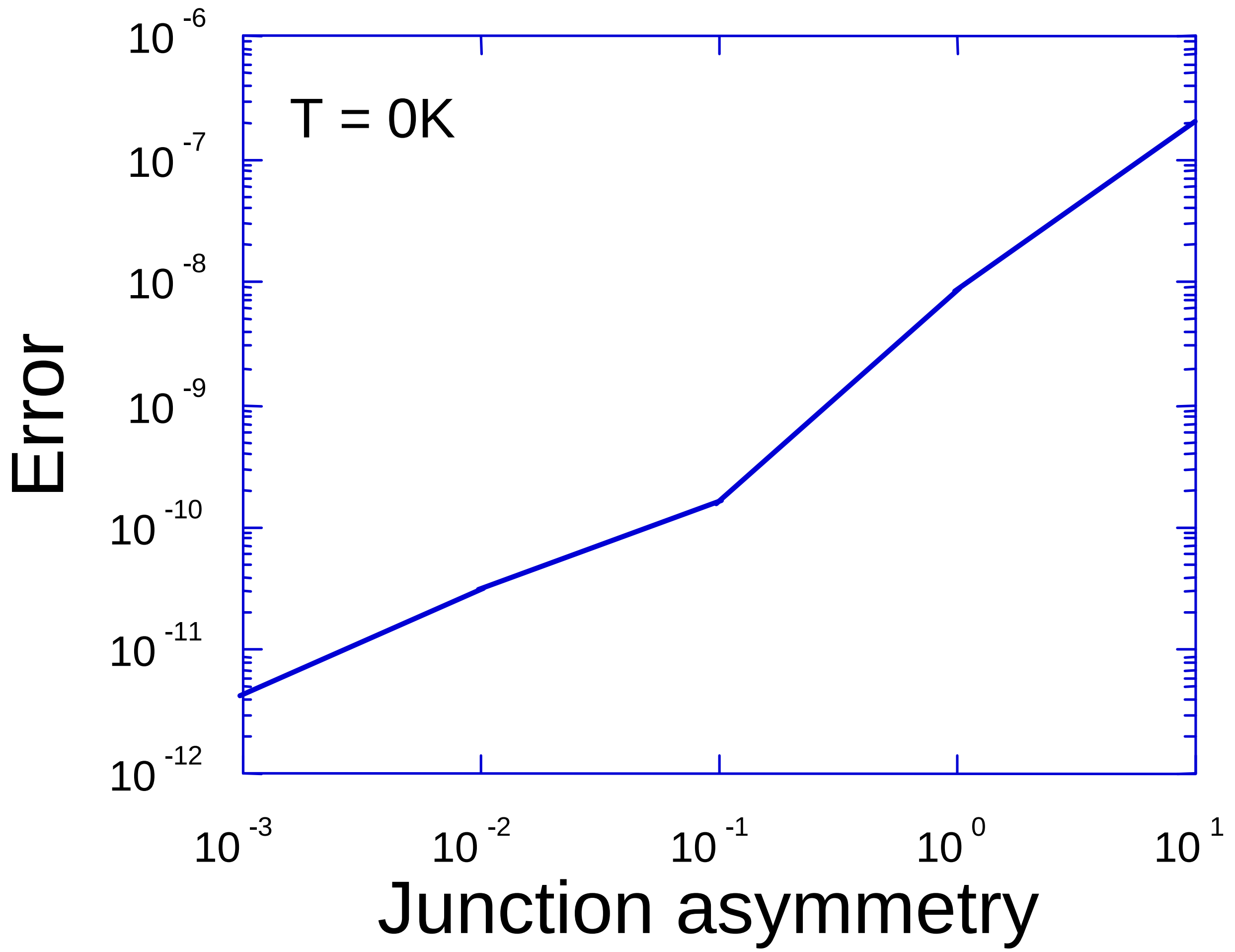
Pump ... Shift register ... Switch

→

Screening length increasing

- Introduce quantum effects and defects for predictive modeling
- Optimize and fabricate building blocks for information processing
  - Shift register, Electron switch

Tunnel Barrier Asymmetry

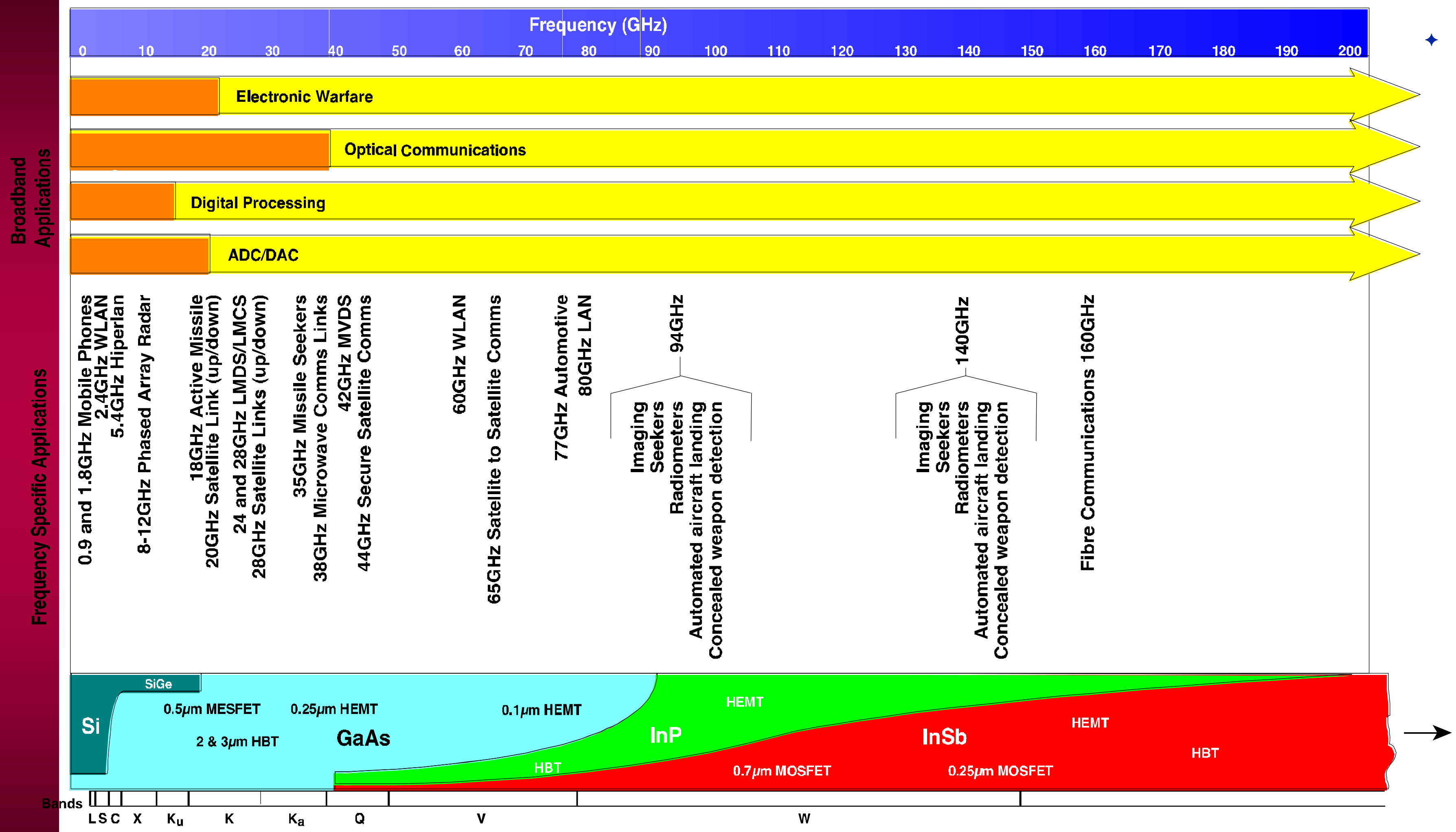


Require flexibility of compound semiconductor heterostructures

Human Knowledge

- One color photo ~ 10^5 b
- Average book ~ 10^6 b
- Average DARPA Program ~10^7 b
- Genetic code ~ 10^{10} b
- Human brain ~ 10^{13} b
- Annual newspapers ~ 10^{14} b
- Selling DARPA Program ~ 10^{14} b
- Library of Congress ~ 10^{15} b
- Human culture ~ 10^{16} b
- Annual television ~ 10^{18} b

Total ~ 10^{19} bytes



Frequency (GHz)

0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170 180 190 200

Broadband Applications

- Electronic Warfare
- Optical Communications
- Digital Processing
- ADC/DAC

Frequency Specific Applications

- 0.9 and 1.8GHz Mobile Phones
- 2.4GHz WLAN
- 5.4GHz Hiperlan
- 8-12GHz Phased Array Radar
- 18GHz Active Missile
- 20GHz Satellite Link (up/down)
- 24 and 28GHz LMDS/LMCS
- 28GHz Satellite Links (up/down)
- 35GHz Missile Seekers
- 38GHz Microwave Comms Links
- 42GHz MVDS
- 44GHz Secure Satellite Comms
- 60GHz WLAN
- 65GHz Satellite to Satellite Comms
- 77GHz Automotive
- 80GHz LAN
- 94GHz
  - Imaging
  - Seekers
  - Radiometers
  - Automated aircraft landing
  - Concealed weapon detection
- 140GHz
  - Imaging
  - Seekers
  - Radiometers
  - Automated aircraft landing
  - Concealed weapon detection
- Fibre Communications 160GHz

Si

SiGe

GaAs: 0.5μm MESFET, 0.25μm HEMT, 0.1μm HEMT, 2 & 3μm HBT

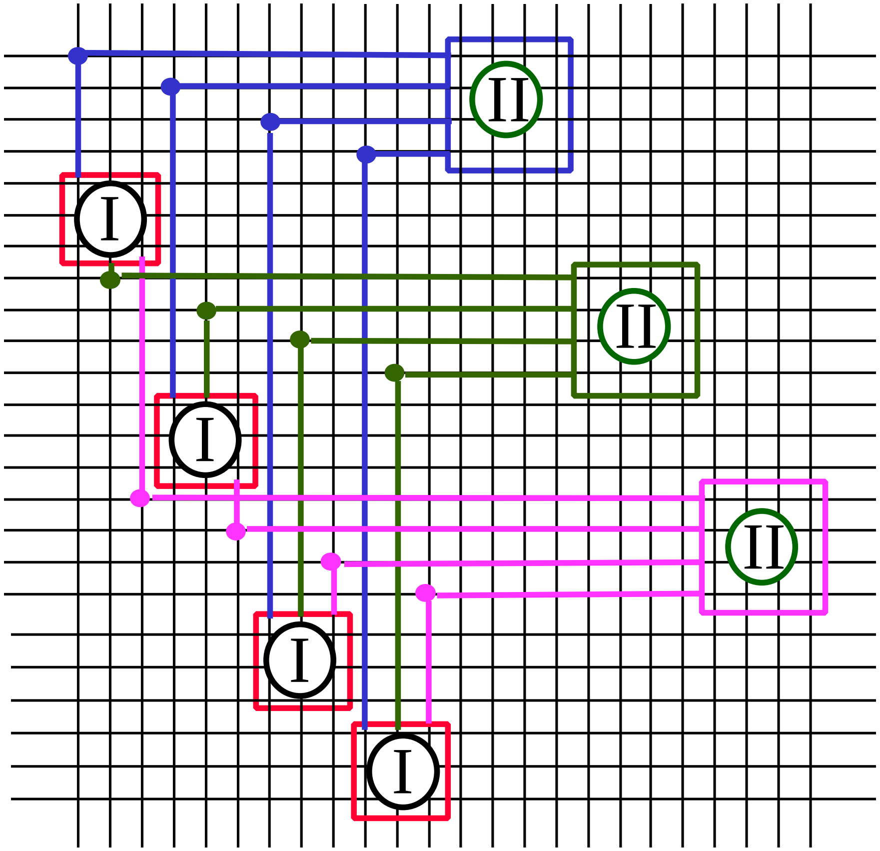
InP: HEMT, HBT

InSb: HEMT, HBT, 0.7μm MOSFET, 0.25μm MOSFET

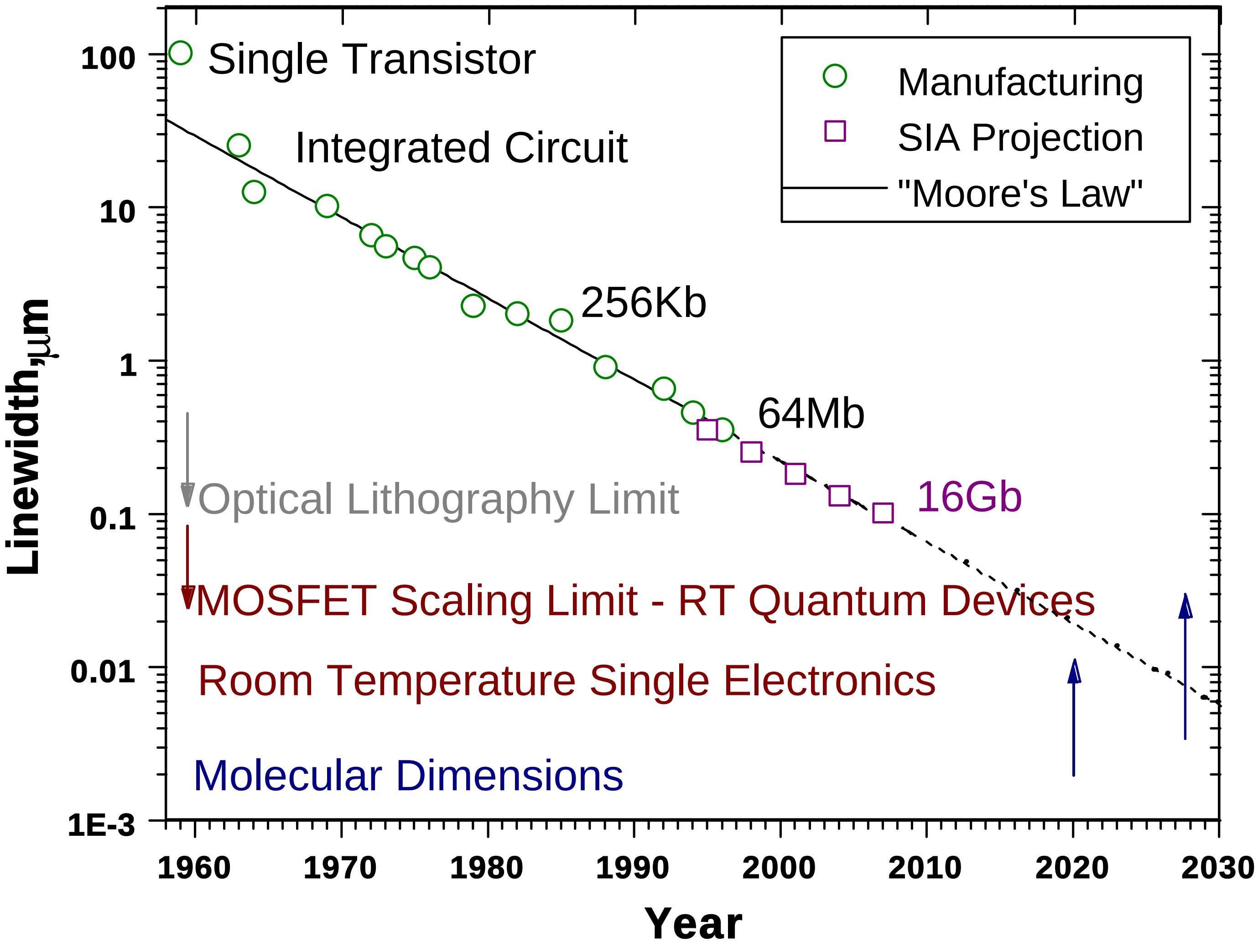
Bands: L S C X K$_u$ K K$_a$ Q V W

Towards Enhanced Defect Tolerance

- Many molecules at each crossbar node
- Module redundancy
- Burn/oxidize bad wires



Device Scaling



Development of a 3-D Nanoelectronic Modeling Tool
NEMO-3D

Gerhard Klimeck, R. Chris Bowen, Tom Cwik,
and Timothy B. Boykin*

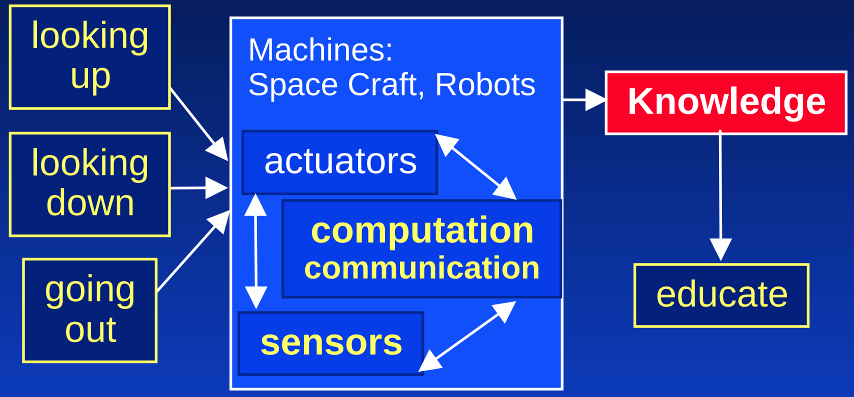
Jet Propulsion Laboratory, California Institute of Technology

*University of Alabama in Huntsville

*Email: gekco@jpl.nasa.gov
Phone: (818) 354 2182
Web: http://hpc.jpl.nasa.gov/PEP/gekco

Revolutionary Computing and Sensing are Enabled by Nanoelectronics

4 Basic NASA Missions: Enabled by Technology



looking up

looking down

going out

Machines:
Space Craft, Robots

actuators

computation
communication

sensors

Knowledge

educate

Example NASA Mission Requirements:
- Autonomous spacecraft
- In-situ data analysis
- On-board image processing

=> Beyond existing system technology

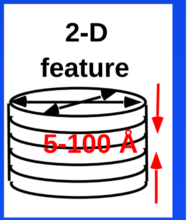
Device/System Requirements:
- Low power and weight, however massive computing and sensing
- Radiation hard devices

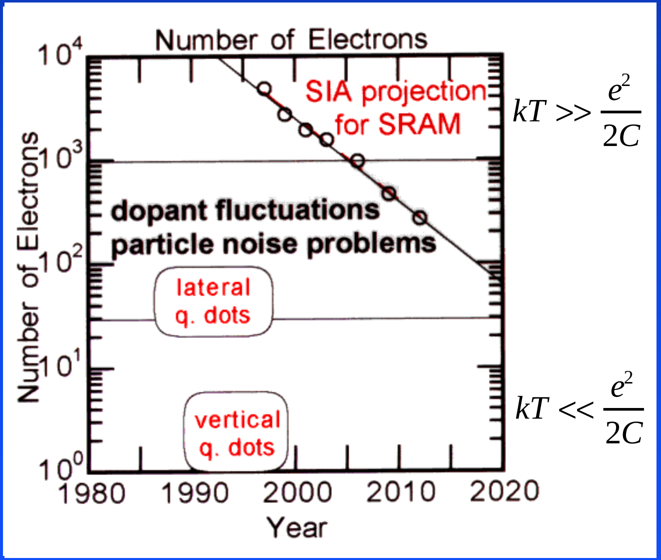
=> Beyond existing device technology

Nanoelectronics:
- Don’t fight, **utilize** quantum behavior:
  - Quantized charge
  - Quantized energy
- Artificial Atoms & Molecules
- Custom optical transitions
- New computation architectures

=> Bottom-up 3-D, atomistic device simulation

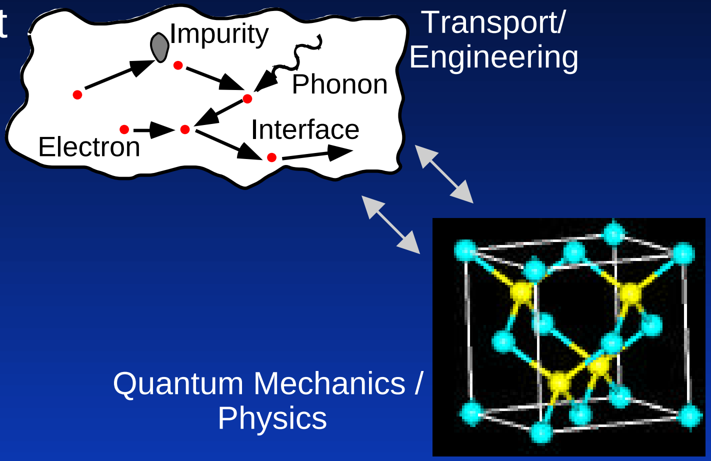
Another Look at Moore’s Law





Leverage NEMO 1-D:
A User-friendly Quantum Device Design Tool

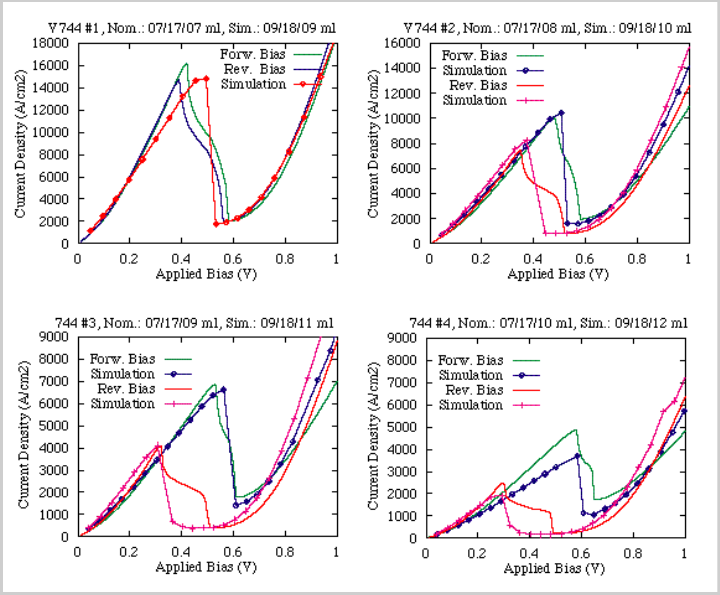
- NEMO was developed under a government contract to Texas Instruments and Raytheon from 1993-97
  - >50,000 person hours of R&D
  - 250,000 lines of code in C, FORTRAN and F90
- NEMO in THE state-of-the-art heterostructure design tool.
- Used at Intel, Motorola, HP, Texas Instruments, and >10 Universities.

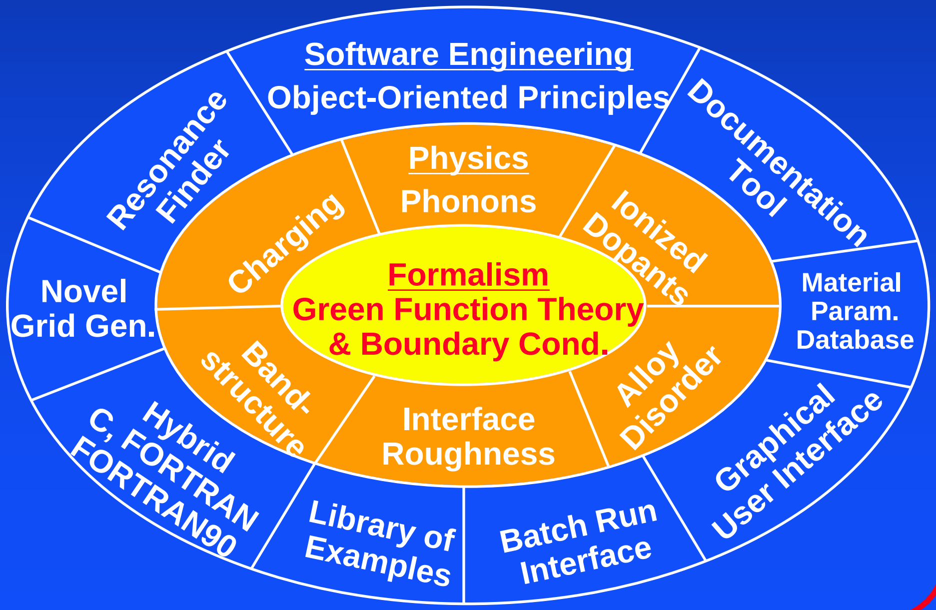


Transport/
Engineering

Quantum Mechanics /
Physics

Testmatrix





Software Engineering
Object-Oriented Principles

Documentation Tool

Material Param. Database

Graphical User Interface

Batch Run Interface

Library of Examples

Hybrid C, FORTRAN FORTRAN90

Novel Grid Gen.

Resonance Finder

Physics
Phonons

Ionized Dopants

Alloy Disorder

Interface Roughness

Band-structure

Charging

Formalism
Green Function Theory & Boundary Cond.

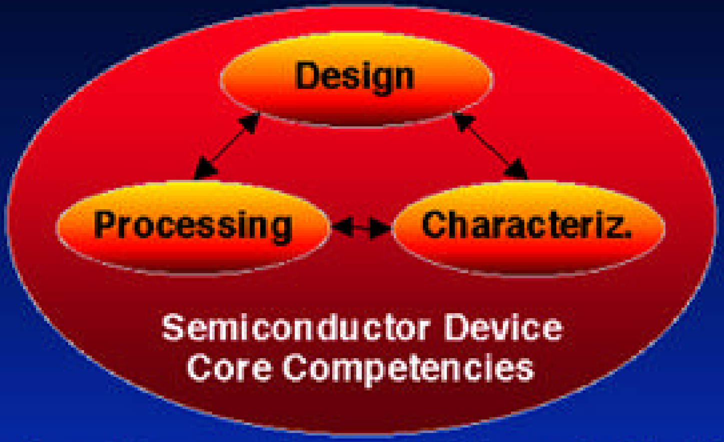
How do you know what you built?

NEMO 1-D used as Device Characterization Tool

Design:
- Circuit and device simulation is a standard tool in industry.
- Only one quantum device design tool: NEMO.

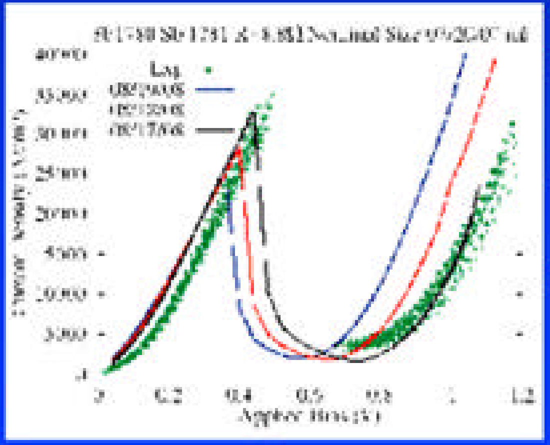
Characterization:
- Few non-destructive tools are available on the nanometer scale.
- Modeling starts to show impact!

Processing:
- Models are in their infancy.



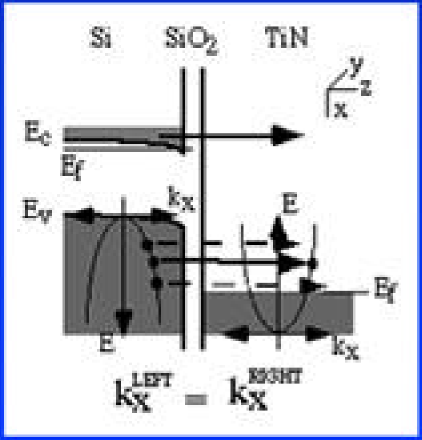
Design, Processing and Characterization are inseparable

NEMO 1-D Usage (Raytheon/TI/JPL)



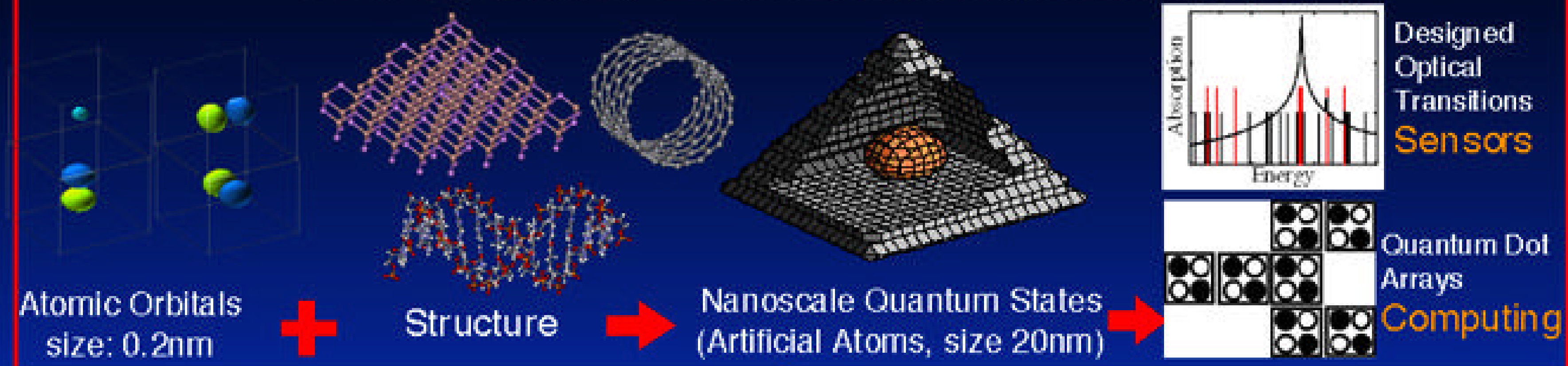
- Monolayer Sensitivity -> characteriz.
- **Genetic Algorithm SYNTHESIS / ANALYSIS**

NEMO 1-D CMOS Characterization (TI)



- Standard: Oxide thickness from capacitance.
- Thin SiO_2 (2nm) is leaky.
- $G > \omega C$
- **New:** oxide thickness from tunneling sim.

Quantum Dot Simulation for Revolutionary Computing and Sensing



Atomic Orbitals
size: 0.2nm

+

Structure

→

Nanoscale Quantum States
(Artificial Atoms, size 20nm)

→

Designed
Optical
Transitions
Sensors

Quantum Dot
Arrays
Computing

Opportunity:
- Nanoscale electronic structures can be built!
  => Artificial Atoms / Molecules

Problem:
- The design space is huge: choice of materials, compositions, doping, size, shape.

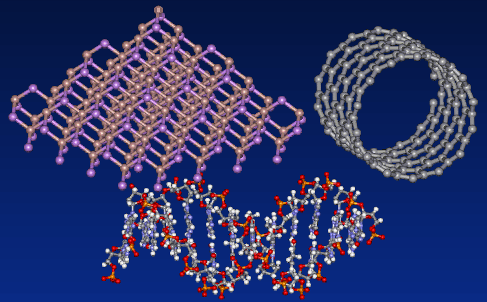
Approach:
- Deliver a 3-D atomistic simulation tool
- Enable analysis of arbitrary crystal structures, atom compositions and bond/structure configurations.

NASA Relevance:
- 2-5μm Lasers and detectors
- High density, low power computation (logic and memory)
- Life signature biosensors

Impact:
- Low cost development of revolutionary technology.
- Narrow empirical/experimental search space

Collaborators:
- Ames, University of Alabama-Huntsville, Purdue

Dissimilar Compounds Experience Strain!
Strain Modifies Electronic Characteristics!



Structure

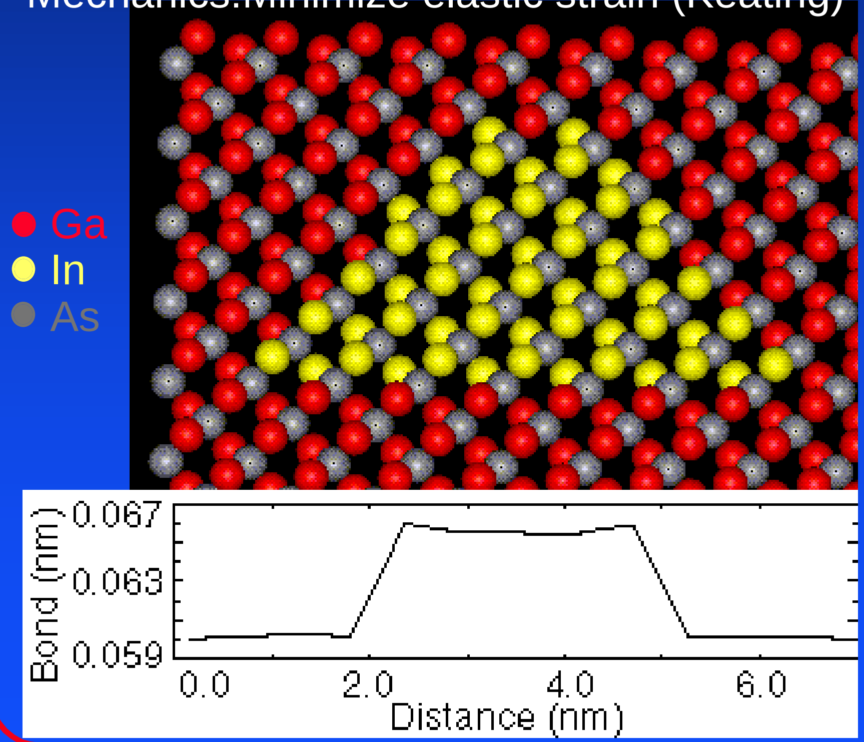
Dot Formation Due to Strain:

- Self-Assembly induced by strain in GaAs/InAs and Si/Ge material systems.
- Bond length and orientation distortion

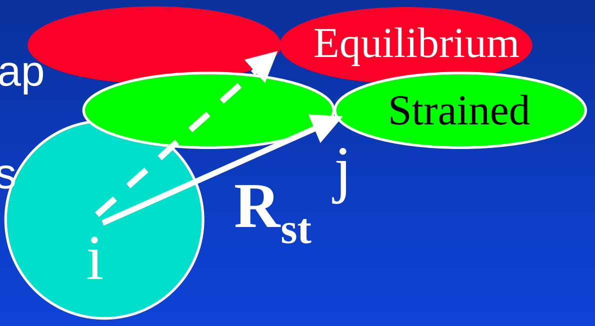
Strain affects Electronic Structure:

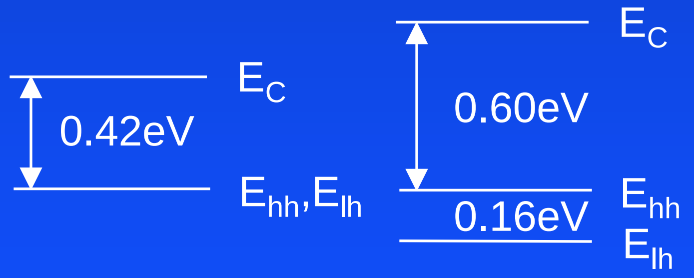
- Tight binding models can predict this!

Mechanics:Minimize elastic strain (Keating)



Electronics:
Orbital overlap changes
=> bandgaps and masses

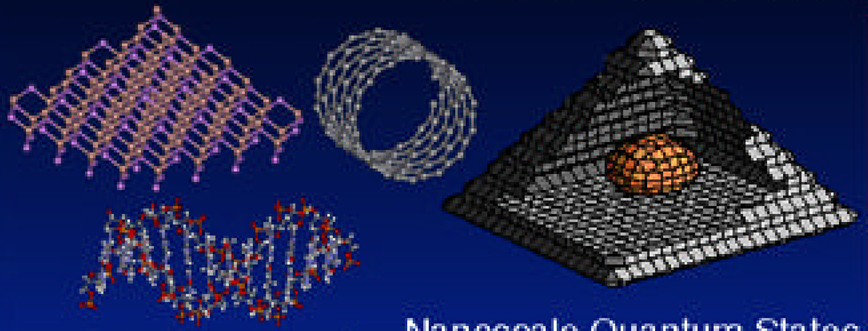




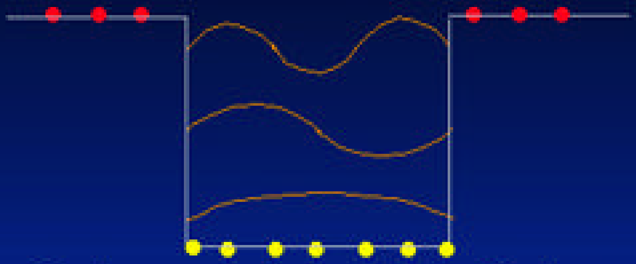
InAs at 4K in GaAs/InAs/GaAs superlattice,
Brühbach et al, Superlatt.&Microstr. V21, n.4 (1997)

Dissimilar Materials Create Quantum Confinement

Nanoscale Quantum States Emerge



Structure → Nanoscale Quantum States (Artificial Atoms, size 20nm)



Objective:

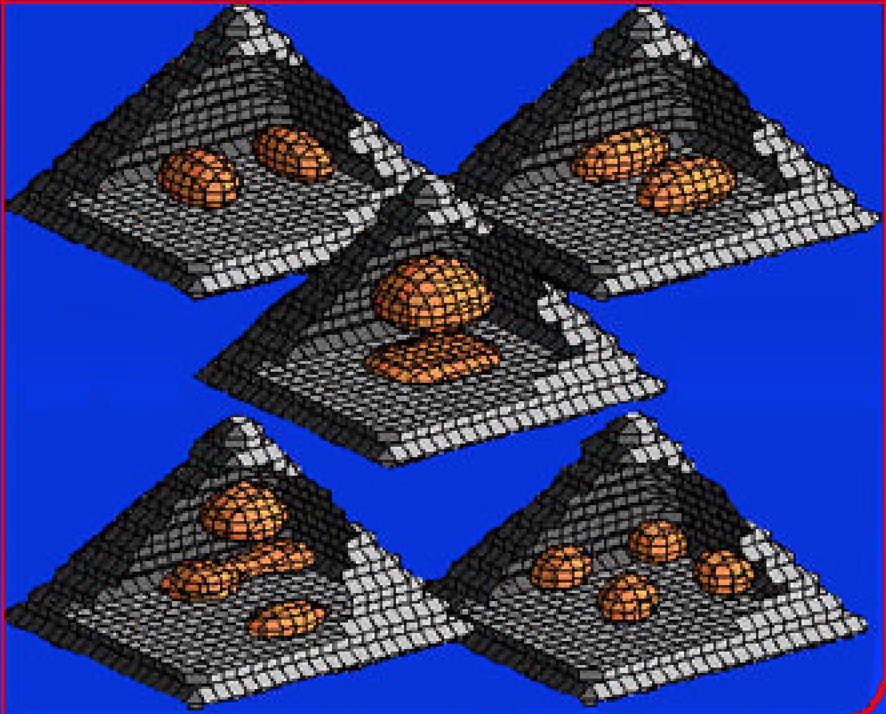
- Need to locate new quantum state energies and wave functions.

Problem:

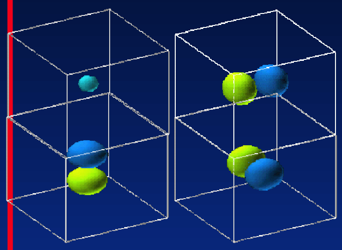
- Realistic Quantum Dots consist of about 10^6 atoms
- Realistic system is OPEN

Approach:

- Custom Lanczos Eigenvalue Solver for Hermitian and non-Hermitian Matrices
- Massively parallel implementation.

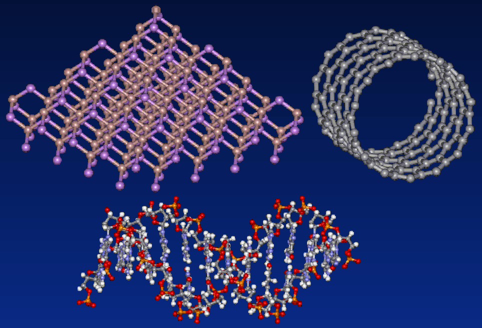


Mapping of Orbitals to Bulk Bandstructure



Atomic Orbitals
size: 0.2nm

+



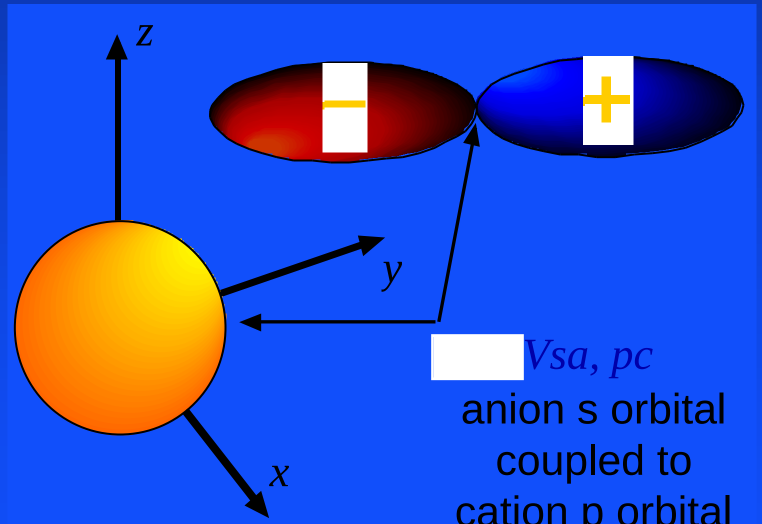
Structure

Bulk Semiconductors are described by:

- Conduction and valence bands, bandgaps (direct, indirect), effective masses
- 10-30 physically measurable quantities

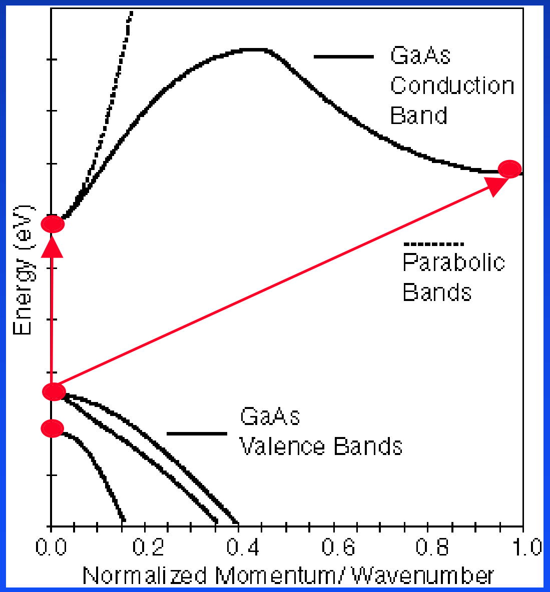
Tight Binding Models are described by:

- Orbital interaction energies.
- 15-30 theoretical parameters



anion s orbital
coupled to
cation p orbital

High
Dimensional
Fitting
Problem



15-30 theoretical interaction energies

10-30 data points of bands and masses

Global Optimization using Genetic Algorithms

Utilizing Evolutionary Principles of Survival of the Fittest

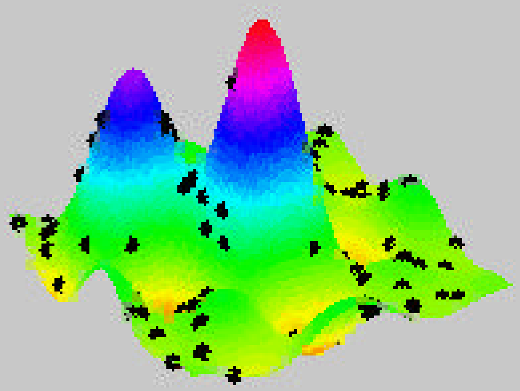
Genetic Algorithm Overview:

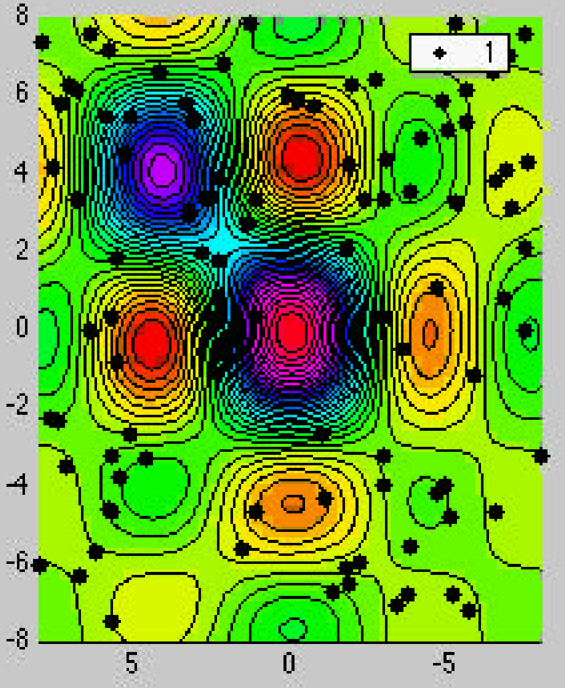
Stochastic placement of individuals in the search/design space.

Every Generation eliminate “unfit” elements and create new ones from survivors.

Reevaluate the fitness of population.

$$F(x,y)=\frac{\sin(x)}{x}\frac{\sin(y)}{y}+0.7\frac{\sin(x-4)}{(x-4)}\frac{\sin(y-4)}{(y-4)}$$





pop = 100, 300 generations, steady-state (10%), 2-point crossover p = 0.85, mutatation p = 1/2

Genetically Engineered Nanoelectronic Structures (GENES)

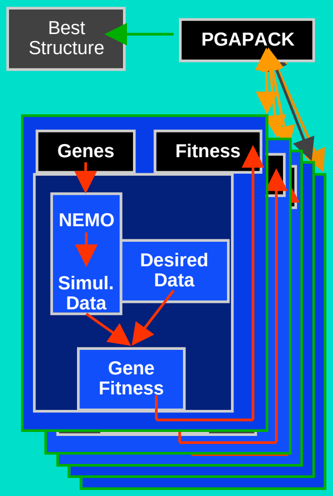
Objectives:

- Automate nanoelectronic device synthesis, analysis, and optimization using genetic algorithms (GA).

Approach:

- Augment parallel genetic algorithm (PGApack).
- Combine PGApack with NEMO.
- Develop graphical user interface for GA.
- GA analyzed atomic monolayer structure and doping profile of RTD device

Architecture



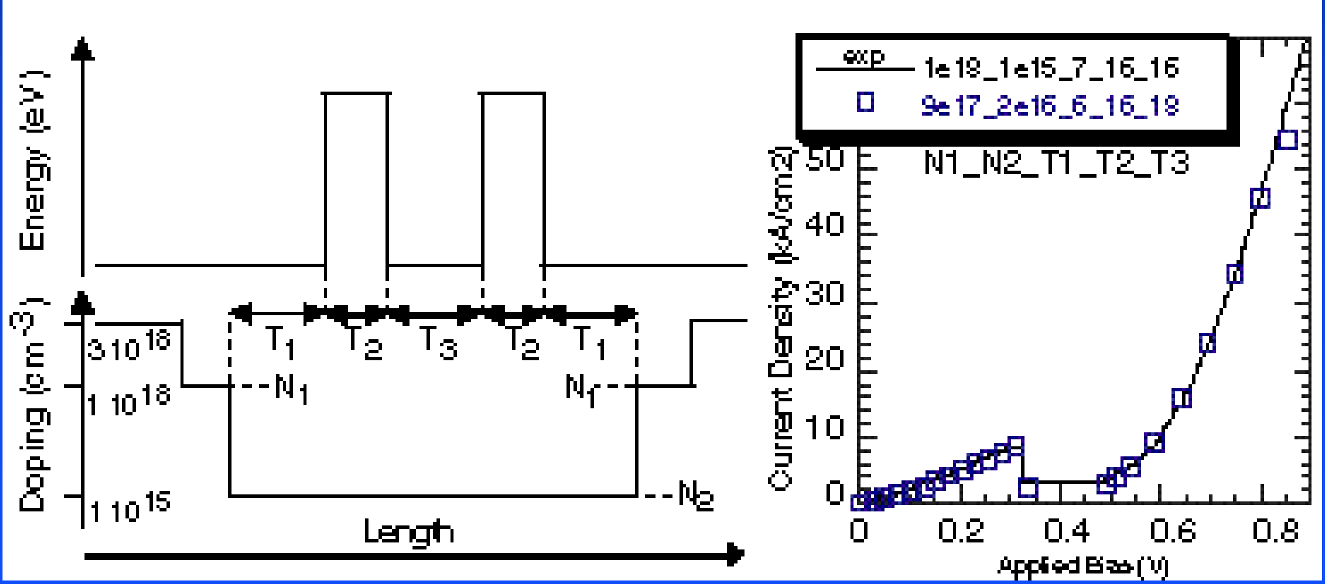
Software Package with Graphical User Interface

Input:
- **Simulation Targets**
- **GA parameters**
- **Platform parameters**
- **Interaction between workstation/PC and supercomputer**

Output:
- **Evolution development**
- **Evolution results**
- **Evolution statistics**

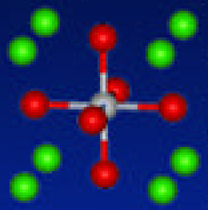
Results:

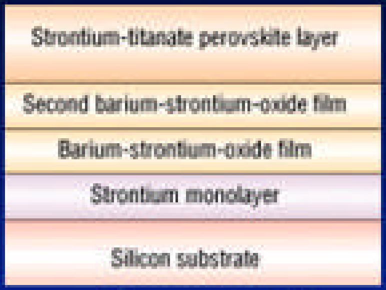
Nanoelectronic Device Structural analysis



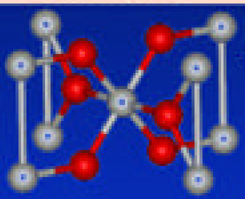
SoC/Mult-Chip-Modules of the Future?
There is a place for atomistic device simulation!

$(Ba,Sr)TiO_3$



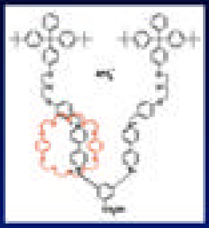


CMOS
Advanced Gate Dielectrics

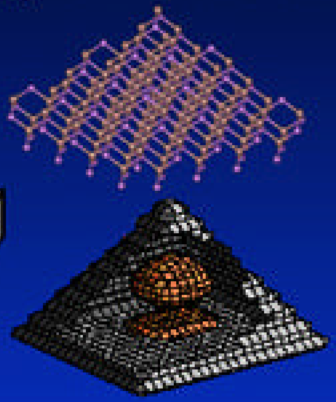


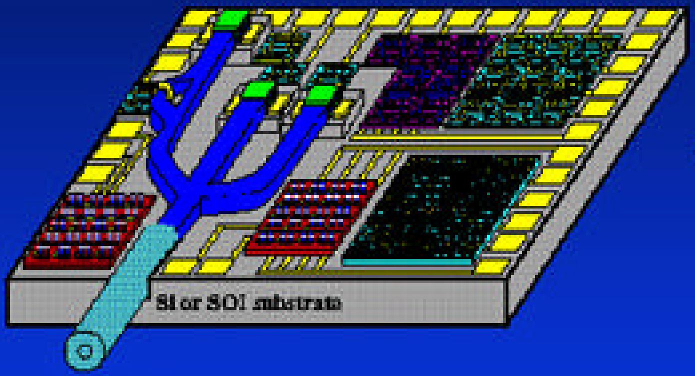
TiO_2

Molecular Switch

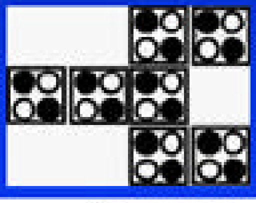


Quantum Dot Optical Detectors

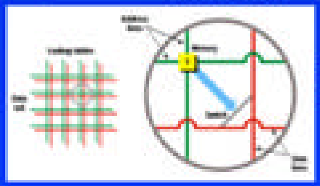




Alternative Architectures

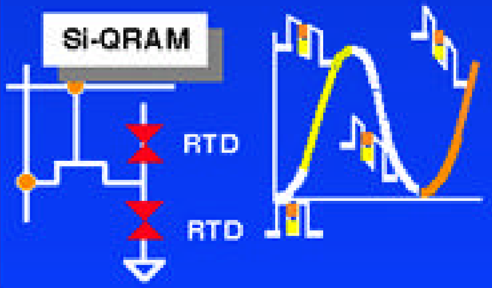


Quantum Cellular Automata

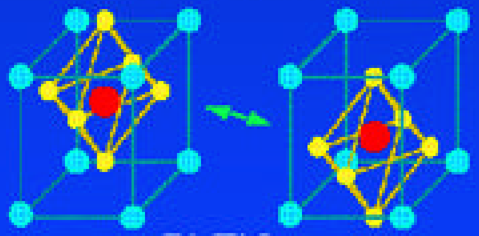


Molecular Teramac

QRAM
High Density Static



FRAM
Non-volatile Ferroelectric



$PbTiO_3$

gekco

High Performance Computing Group

Heterogeneous Technology Integration and Opportunities in System Design

Krishna C. Saraswat & Robert W. Dutton (speaker)
Stanford University
Center for Integrated Systems

- Motivation
- Fundamental Challenge(s):
  - Rent’s Rule
  - Thermal (and Power)
- 3D IC Technology:
  - Single Chip
  - Multi-Chip (viable alternative)
- Potential Breakthroughs
- Future Design Issues
  (and need for tools)...

Motivation--Systems on a Chip (SoC)

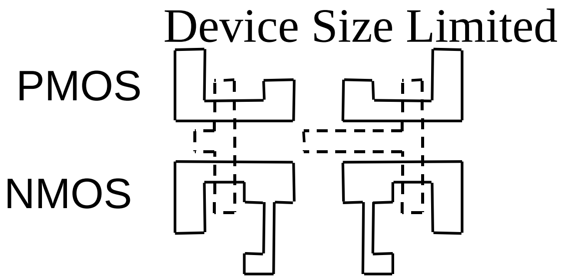
- Digital CMOS will be the “engine” (and chassis) with DSP as essential “fabric” to handle heterogeneous technology used in SoC

- Mixed technology brings host of problems:
  - A/D interfaces
  - Analog design and verification
  - Scaling…not on ITRS and many fundamentally different (“laws”)

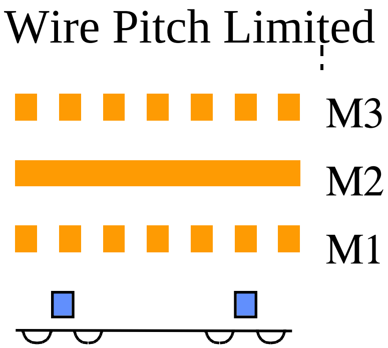
- Cost of chip area on (giga-scale) digital CMOS fundamentally at odds with typical mixed technology components/sub-systems

Chip Size--Memory, Logic & **Analog**

Heterogeneous Technology Blocks have fundamentally different **scaling laws, area constraints** and **system integration issues...**

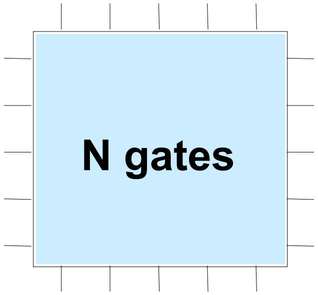


- Memory: SRAM, DRAM



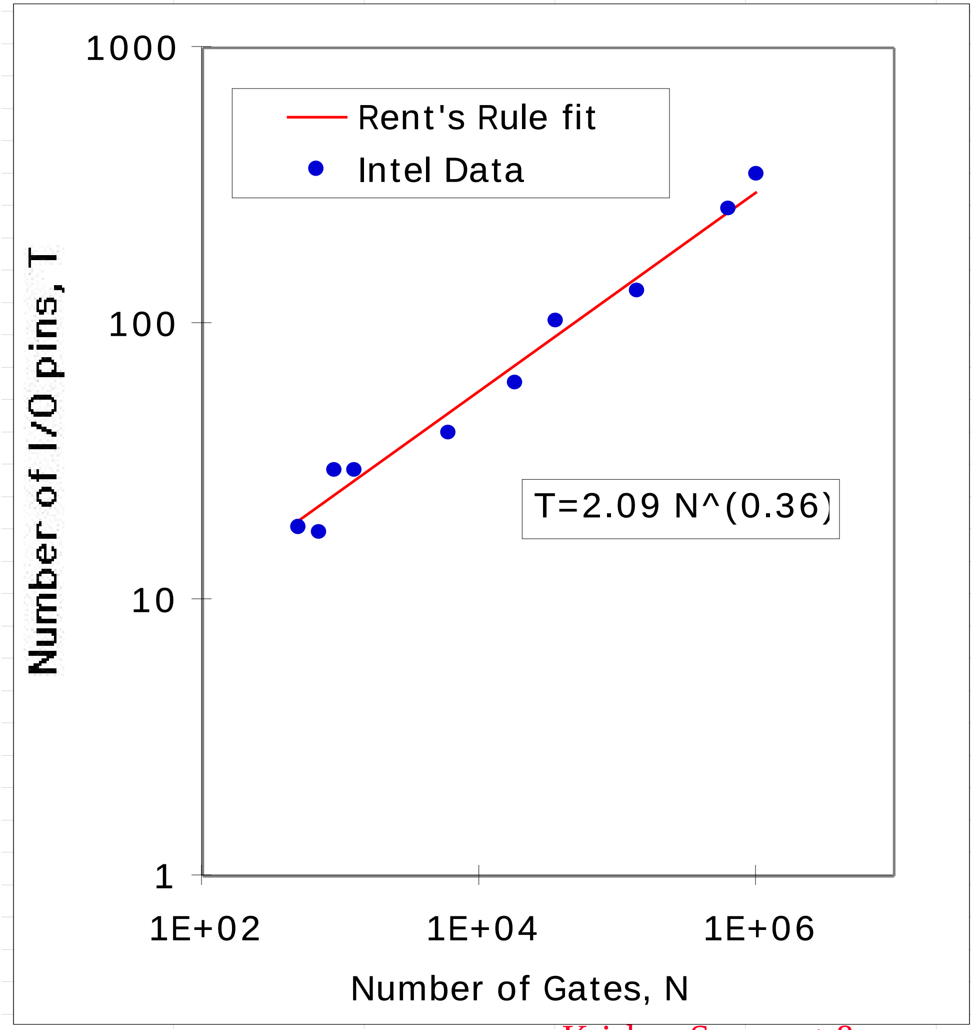
Logic, e.g., µ-Processors

Rent’s Rule



$$T = k\,N^{P}$$

T = # of I/O terminals
N = # of gates
k = avg. I/O’s per gate
P = Rent’s exponent



Chip Area Estimation

- Placement of a wire in a tier is determined by some constraint, e.g., maximum allowed RC delay

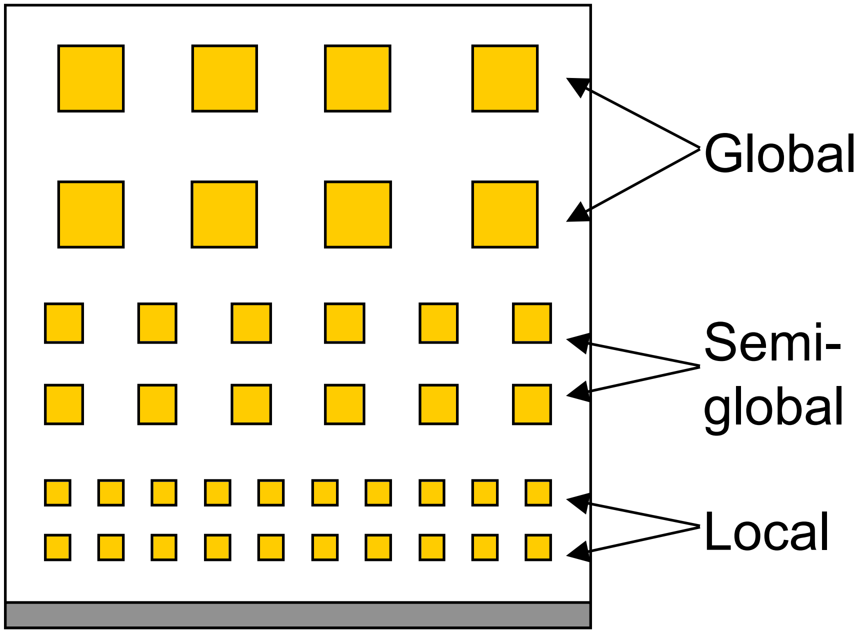
- Wiring Area = wire pitch x total length

$$A_{req} = p_{loc}L_{tot\_loc} + p_{semi}L_{tot\_semi} + p_{glob}L_{tot\_glob}$$
$$= A_{loc} + A_{semi} + A_{glob}$$

- L_{tot} calculated from wire-length distribution

$$A_{chip} = \frac{A_{loc} + A_{semi} + A_{glob}}{\#\ \text{of metal layers}}$$

A 3-tier wiring network



Determination of Wire-length Distribution

- Conservation of I/O's

  $T_A + T_B + T_C = T_{A\text{-to-}B} + T_{A\text{-to-}C} + T_{B\text{-to-}C} + T_{ABC}$

  $T_{A\text{-to-}B} = T_A + T_B - T_{AB}$

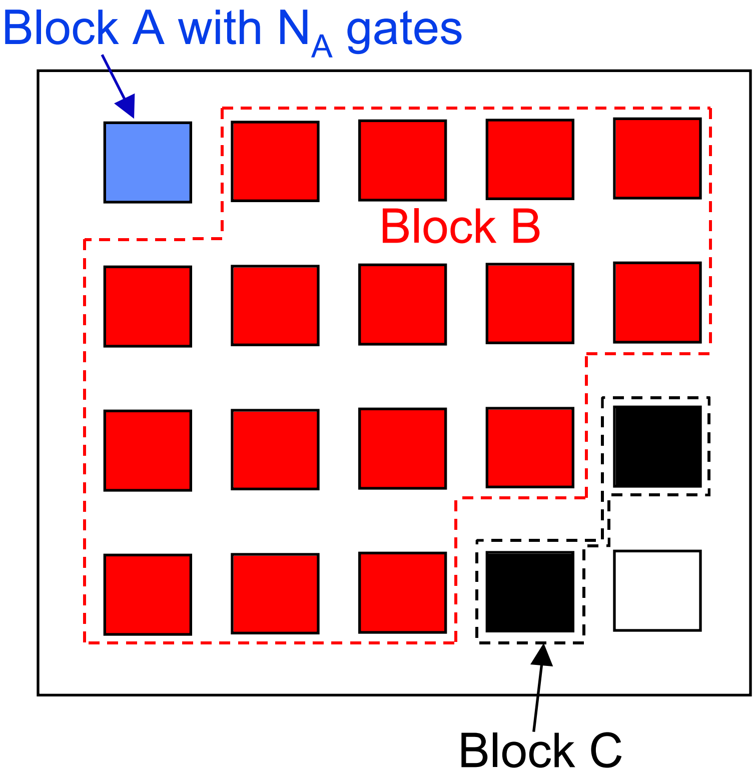
  $T_{B\text{-to-}C} = T_B + T_C - T_{BC}$

- Values of T within a block or collection of blocks are calculated using Rent's rule, e.g.,

  $T_A = k\,(N_A)^P$

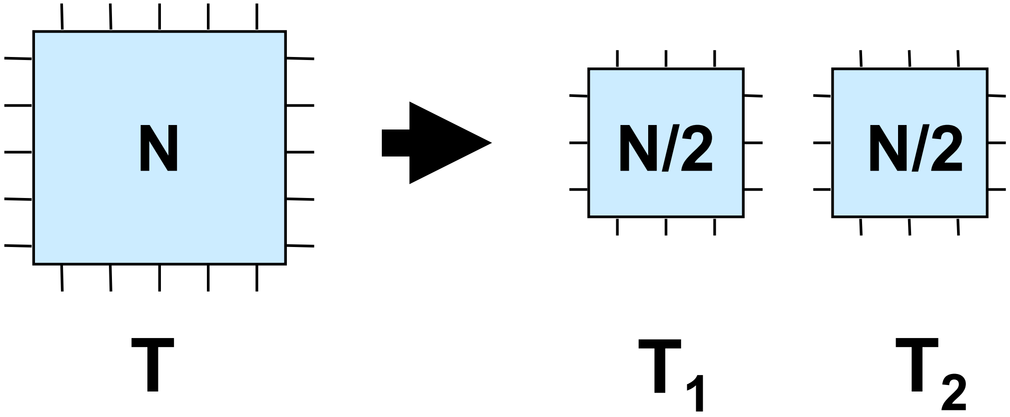
  $T_{ABC} = k\,(N_A + N_B + N_C)^P$

- Recursive use of Rent's rule gives wire-length distribution for the whole chip



Ref: Davis & Meindl, IEEE TED, March 1998

Inter-Layer Connections For 3-D / 2-Layers



- Fraction of I/O ports $\mathbf{T_1}$ and $\mathbf{T_2}$ is used for inter-layer connections, $\mathbf{T_{int}}$
- Assume I/O port conservation:

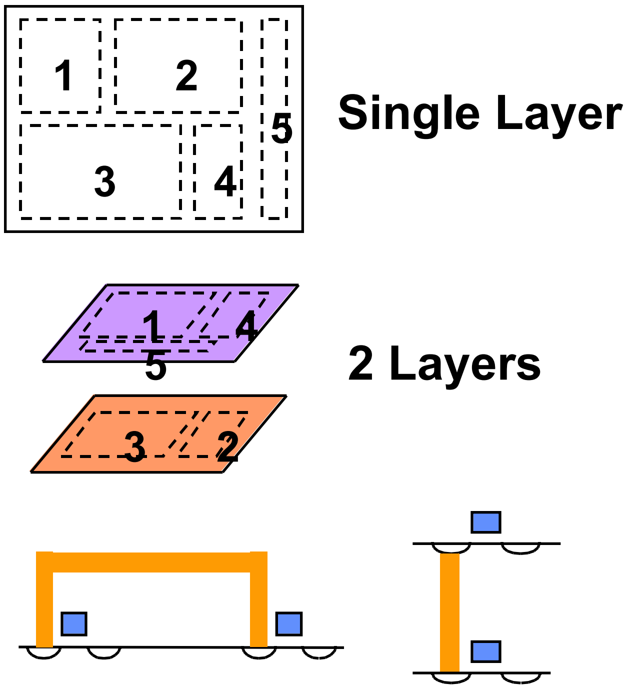
$$\boxed{T = T_1 + T_2 - T_{int}}$$

- Use Rent's Rule: $\mathbf{T = kN^p}$ to solve for $\mathbf{T_{int}}$ (**p** assumed constant)

k = Avg. I/O's per gate **N** = No. of gates **p** = Rent's exponent

Ref: Souri, Banerjee, Mehrotra & Saraswat, **DAC, June 2000**

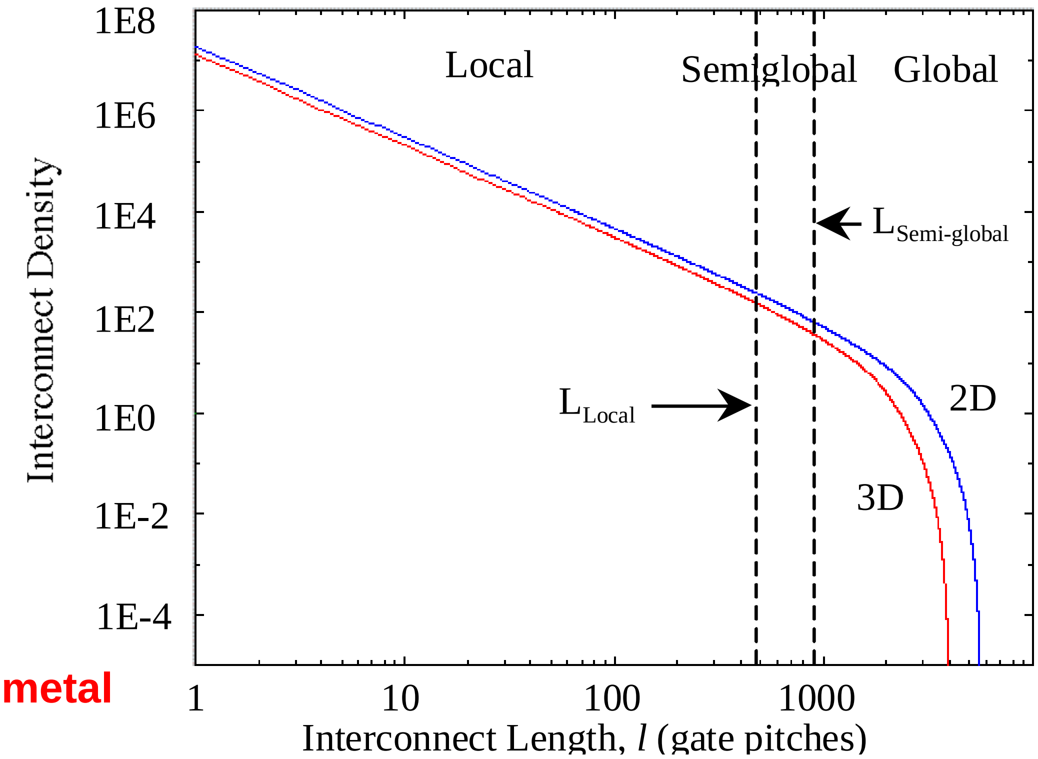
Wire-length Distribution of 3-D IC



Replace horizontal by vertical interconnect

Microprocessor Example from NTRS 50 nm Node

Number of Gates	180 million
Minimum Feature Size	50 nm
Number of wiring levels,	9
Metal Resistivity, Copper	1.673e-6 Ω-cm
Dielectric Constant, Polymer	$e_r = 2.5$

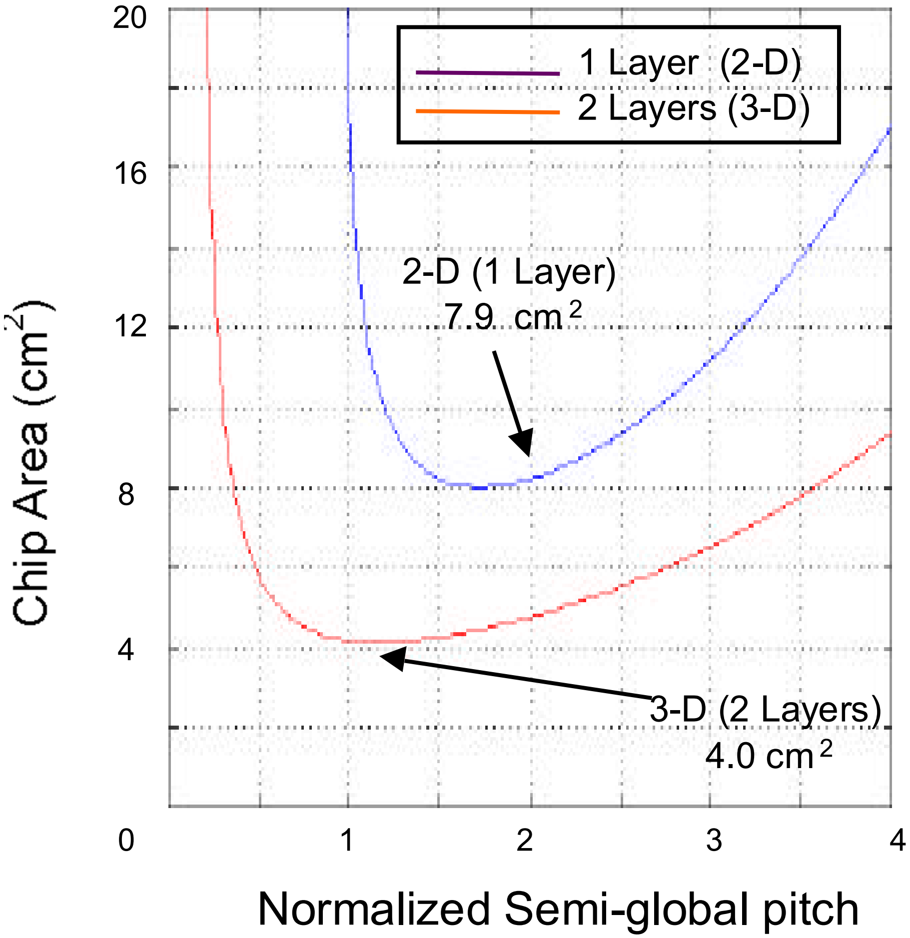


Vertical inter-layer connections reduce metal wiring requirement...

Ref: Souri, Banerjee, Mehrotra & Saraswat, **DAC, June 2000**

2 Active Layer Results

- Upper tiers pitches are reduced for constant chip frequency, f_c
- Less wiring needed
- Almost 50% reduction in chip area

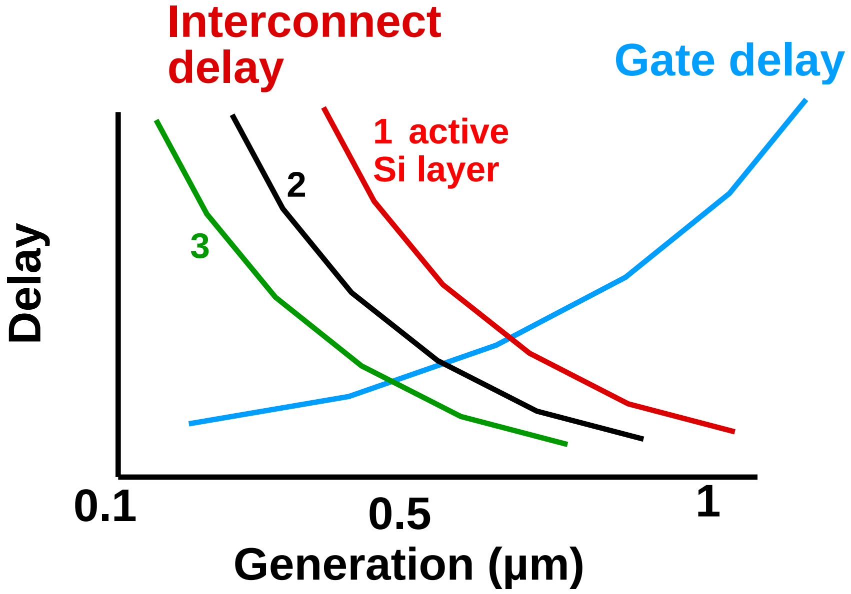


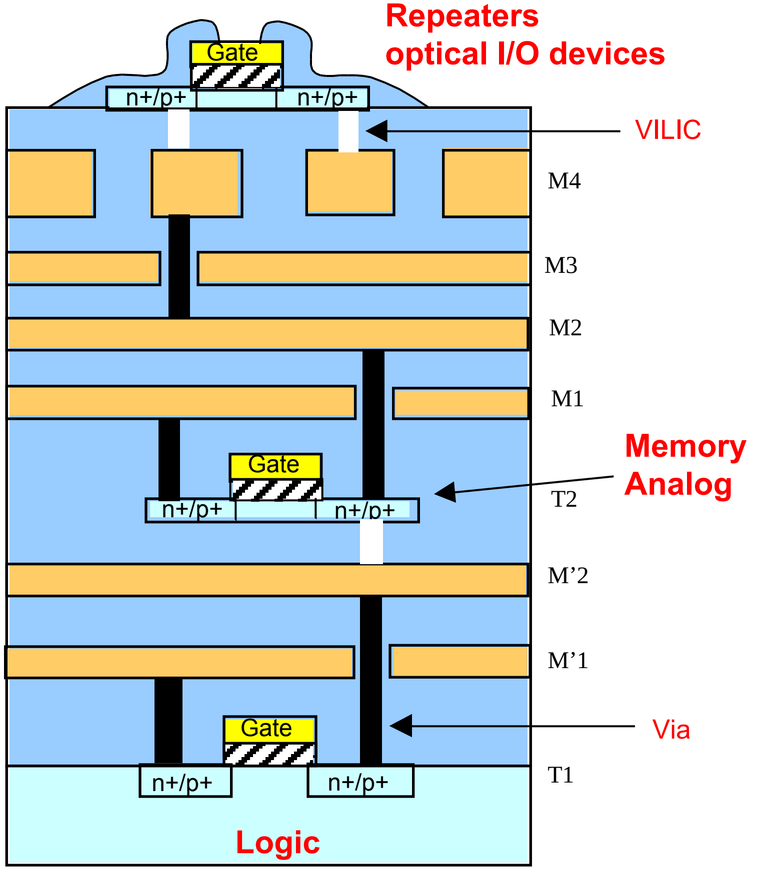
Ref: Souri, Banerjee, Mehrotra & Saraswat, **DAC, June 2000**

3D ICs with Multiple Active Si Layers

Motivation

- Performance of ICs is limited due to R, L, C of interconnects
- Interconnect length and therefore R, L, C can be minimized by stacking active Si layers
- Number of horizontal interconnects can be minimized by using vertical interconnects
- Disparate technology integration possible, e.g., memory & logic, RF, optical I/O, etc.

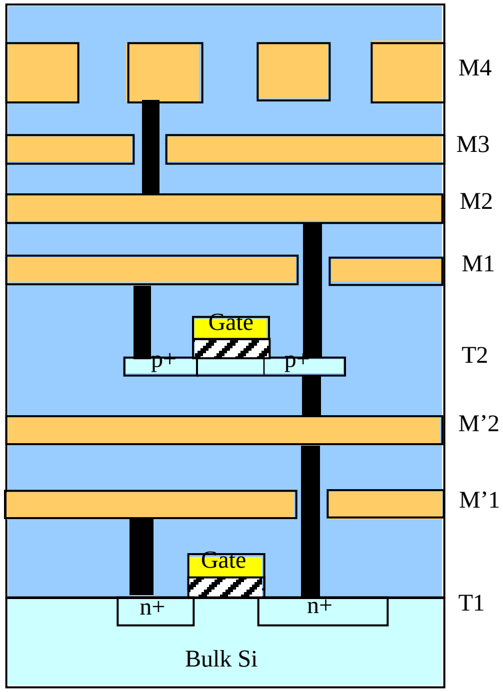


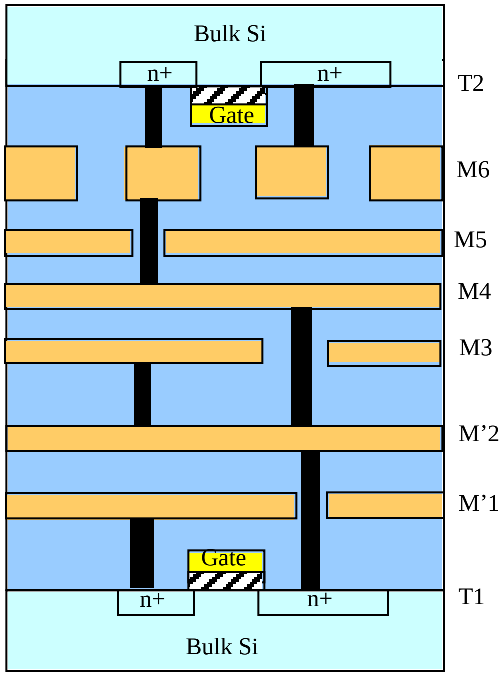


tanford University

Krishna Saraswat &
Bob Dutton (edits/additions)

3D Examples for Thermal Study

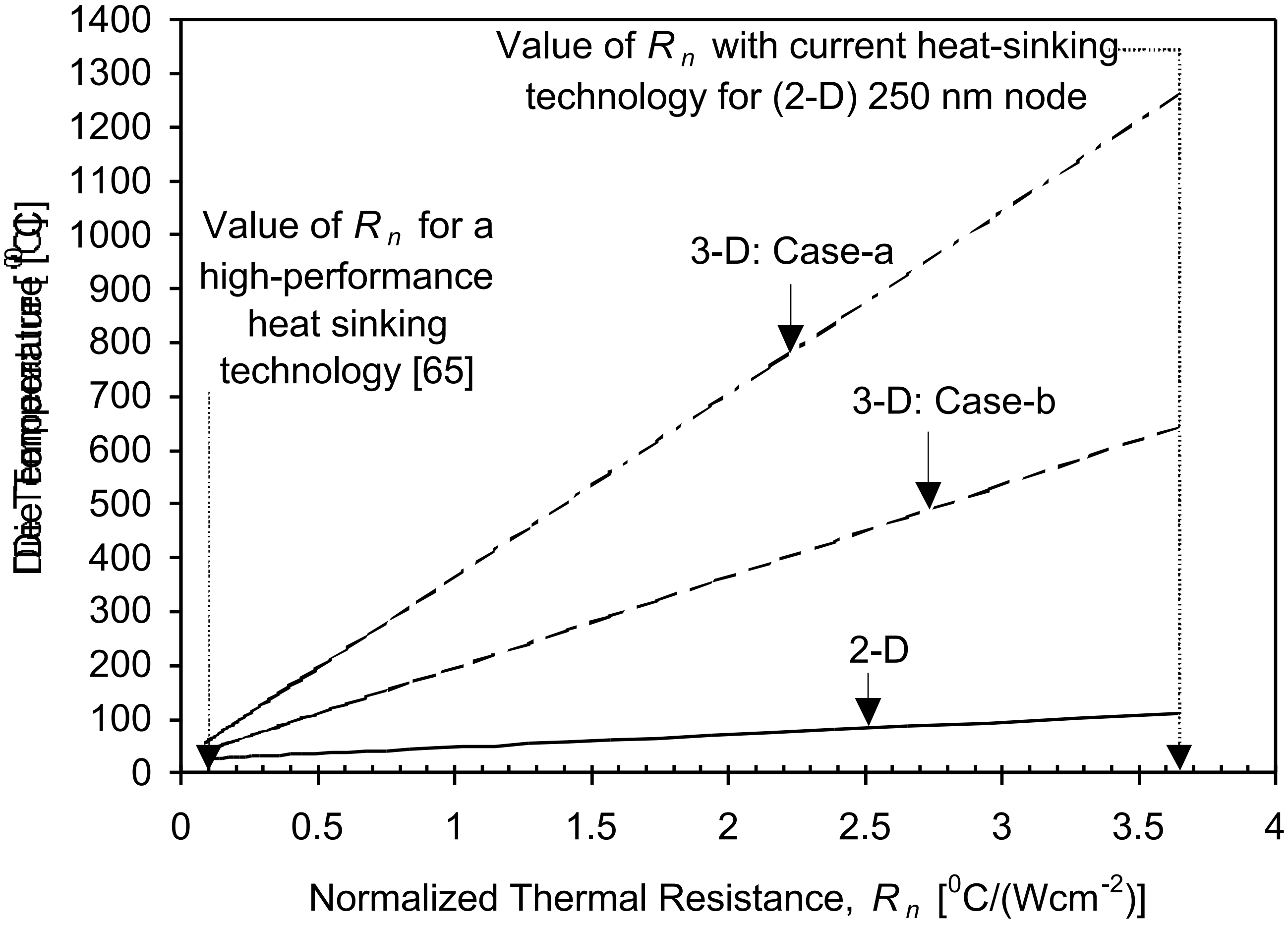




- Case A: Heat dissipation is confined to one surface

- Case B: Heat dissipation possible from 2 surfaces.

Die Temperature Simulation

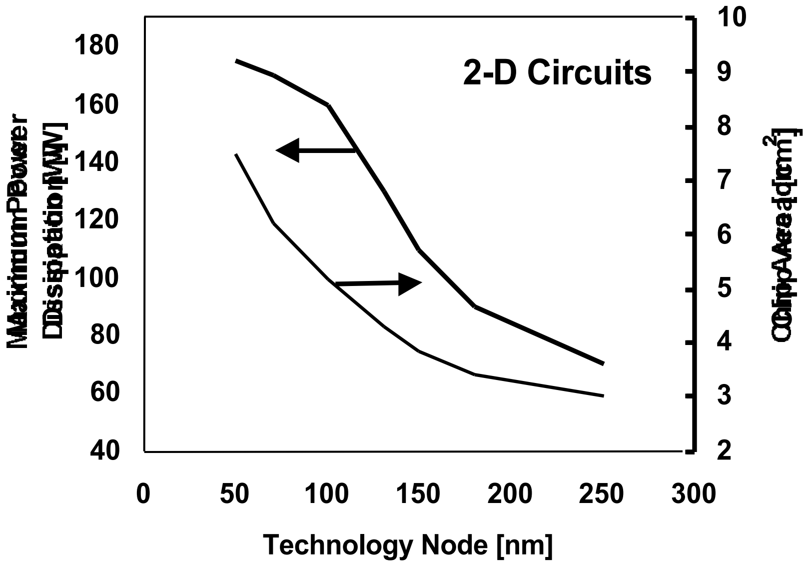


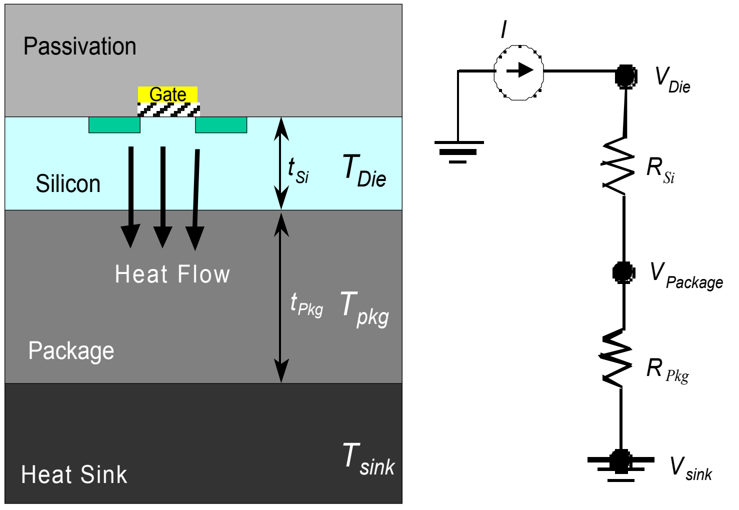
Attainable die temperatures for 2-D and 3-D ICs at the NTRS based 50 nm node using advanced heat-sinking technologies that would reduce the normalized thermal resistance, *R*

Ref: Souri, Banerjee, Mehrotra & Saraswat, **DAC, June 2000**

Thermal Behavior in 3D ICs

Power Dissipation for 2D





a) b)

- Energy is dissipated during transistor operation
- Heat is conducted through the low thermal conductivity dielectric, Silicon substrate and packaging to heat sink
- 1-D model assumed to calculate die temperature

3D ICs: Implications for Circuit Design & CAD

- **Critical Path Layout**: By vertical stacking, the distance between logic blocks on the critical path can be reduced to improve circuit performance.
- **Integration of disparate (and/or heterogeneous) technologies is easier:**
  - **Microprocessor Design**: on-chip caches on the second active layer will reduce distance from the logic and computational blocks.
  - **RF and Mixed Signal ICs**: Substrate isolation (noise) between the digital and RF/analog components can be improved by dividing them among separate active layers - ideal for system on a chip design.
  - **Optical I/O** can be integrated in the top layer
- **Repeaters**: Chip area can be saved by placing repeaters (~ 10,000 for high performance circuits -> 25% area factor) on the higher active layers.
- **Physical Design and Synthesis**: Due to a non-planar target graph (upon which the circuit graph is embedded), placement and routing algorithms, and hence synthesis algorithms and architectural choices, need to be suitably modified.

Presentation for DARPA Next Generation CAD for GigaScale Integration Workshop, Rosslyn, VA

Device Trends and CAD Challenges for Gigascale Integration of Molecular-Scale Switches and Circuits

James C. Ellenbogen, Ph.D.

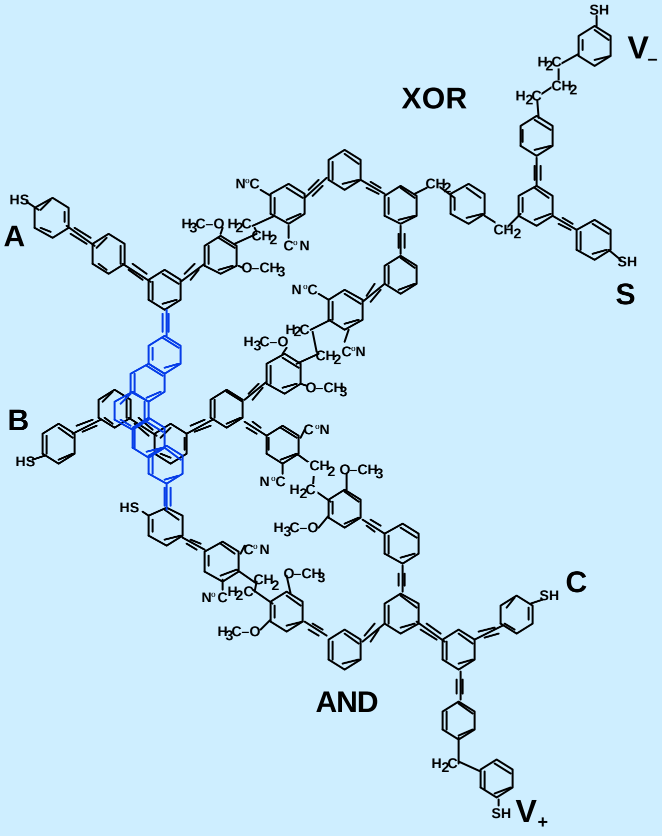
MITRE Nanosystems Group
e-mail: ellenbgn@mitre.org

5 May 2000

MITRE

Basis for this Presentation: MITRE Nanoelectronics R&D

Example: MITRE's Proposed Molecular Electronic Half-Adder



1 million times smaller than comparable circuit on Pentium II

Present Objectives

0 Develop & verify architectures for nanometer-scale electronic computers--*esp., molecular electronic computers*

- Wires, switches, logic structures made from individual molecules
- Compute via passing currents of electrons thru molecules

0 Develop CAD tool for molecular electronics--MolSPICE*

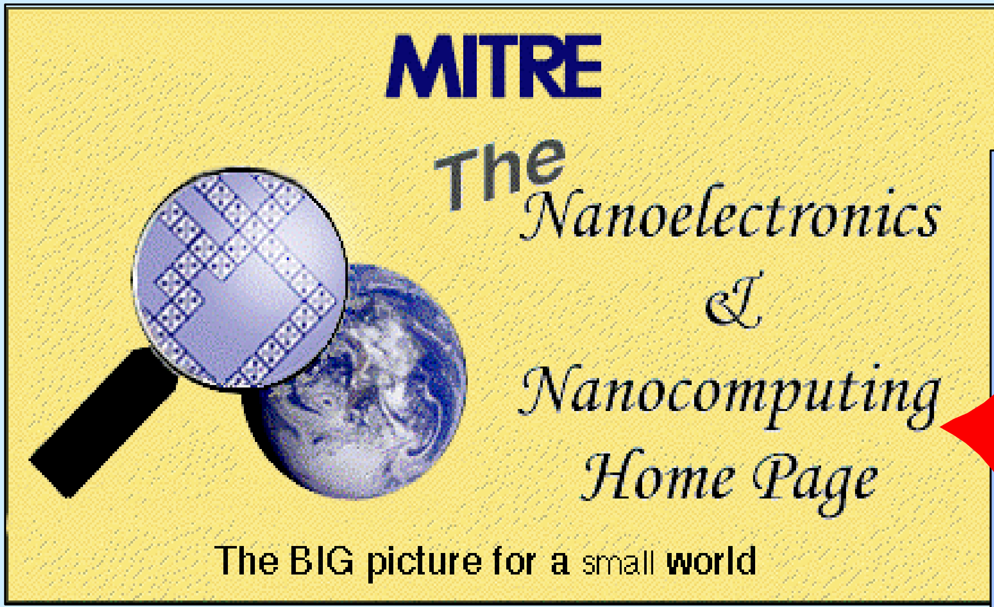
- Design and model molecular circuits
- Including quantum effects

0 Explore fabrication & application concepts for such nanocomputers

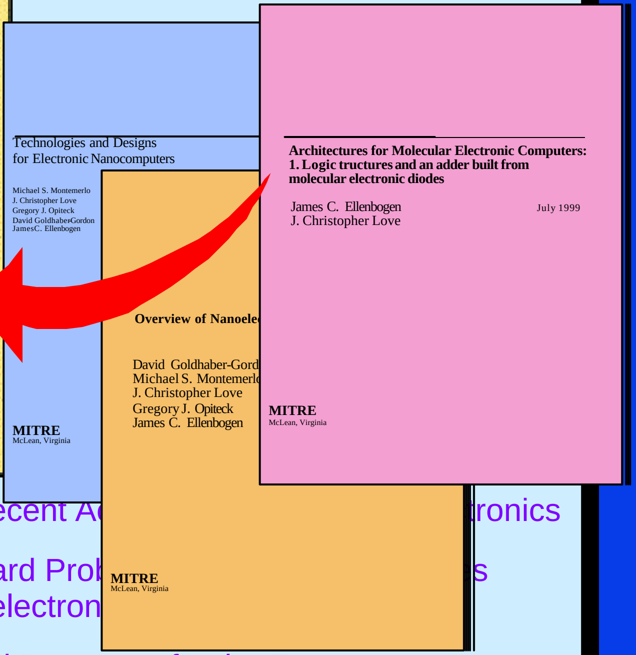
* R&D supported by DARPA Moletronics Program

MITRE

More Nanoelectronics Information on the Internet: Nanoelectronics & Nanocomputing Home Page



Review articles available on Web site



Technologies and Designs for Electronic Nanocomputers

Michael S. Montemerlo
J. Christopher Love
Gregory J. Opiteck
David GoldhaberGordon
JamesC. Ellenbogen

MITRE
McLean, Virginia

Overview of Nanoele

David Goldhaber-Gord
Michael S. Montemerlo
J. Christopher Love
Gregory J. Opiteck
James C. Ellenbogen

MITRE
McLean, Virginia

Architectures for Molecular Electronic Computers: 1. Logic tructures and an adder built from molecular electronic diodes

James C. Ellenbogen
J. Christopher Love

July 1999

MITRE
McLean, Virginia

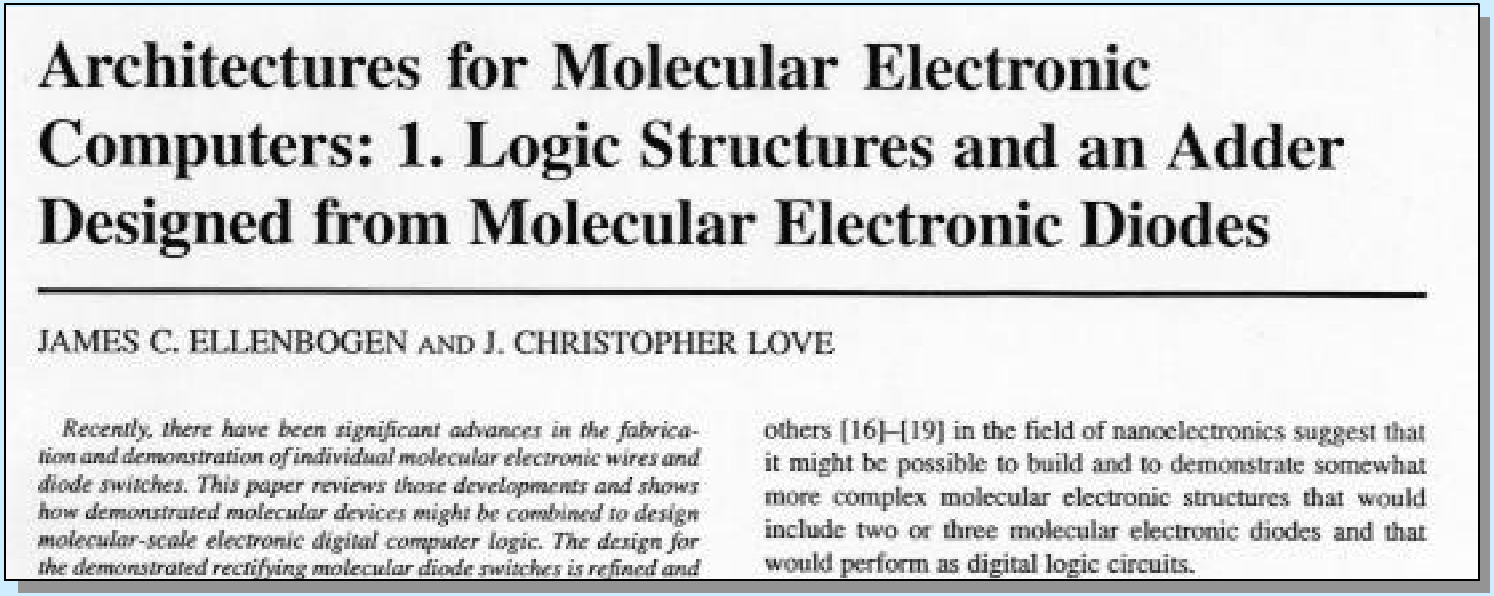
- What are Nanotechnology and Nanoelectronics?
- Basic References on Nanoelectronics and Nanocomputi
- Who's Who in Nanoelectronics and Nanocomputing
- Links to other WWW Sites Relevant to Nanoelectronics
- Top 10 Recent A tronics
- Top 10 Hard Prob s for Nanoelectron
- Status and Prospects for the Future
- *and much more!*

On the Internet at *http://www.mitre.org/technology/nanotech*

MITRE

“Pink Book” Recently Published in March 2000 *Proceedings of the IEEE*

- **Explains basic ideas of molecular electronics and shows what a molecular-scale computer might “look” like**



Architectures for Molecular Electronic Computers: 1. Logic Structures and an Adder Designed from Molecular Electronic Diodes

JAMES C. ELLENBOGEN AND J. CHRISTOPHER LOVE

Recently, there have been significant advances in the fabrication and demonstration of individual molecular electronic wires and diode switches. This paper reviews those developments and shows how demonstrated molecular devices might be combined to design molecular-scale electronic digital computer logic. The design for the demonstrated rectifying molecular diode switches is refined and

others [16]–[19] in the field of nanoelectronics suggest that it might be possible to build and to demonstrate somewhat more complex molecular electronic structures that would include two or three molecular electronic diodes and that would perform as digital logic circuits.

- **Reviews recent experimental and theoretical results in molecular electronics**
- **Proposes designs for molecular logic circuits and functions**

Main Points
of This Presentation

- **<u>Where are we headed:</u>**
  Molecular-scale **devices (~5-50 nm long) in ultra-dense assemblages of devices and <u>circuits</u>**

- **<u>What are the new design challenges (in overview):</u>**
  - **Multiple types of devices (FETs plus quantum-effect switches and circuits) in the same system**
  - **New types of devices--e.g., molecules**
  - **Large numbers of devices without intrinsic gain--diodes**
  - **Quantum mechanics--accounting for it and using it to advantage in circuits, as well as in devices**
  - **New materials with new properties**
  - **Huge numbers of devices (~10^{10} or 10^{12}/mm^2) with novel circuit & system organizations--massive parallelism & 3-D**
  - **Error and fault tolerant architectures**
  - **Heat and interconnects**

FETs = Field Effect Transistors
(i.e., solid-state, bulk-effect microelectronic devices)

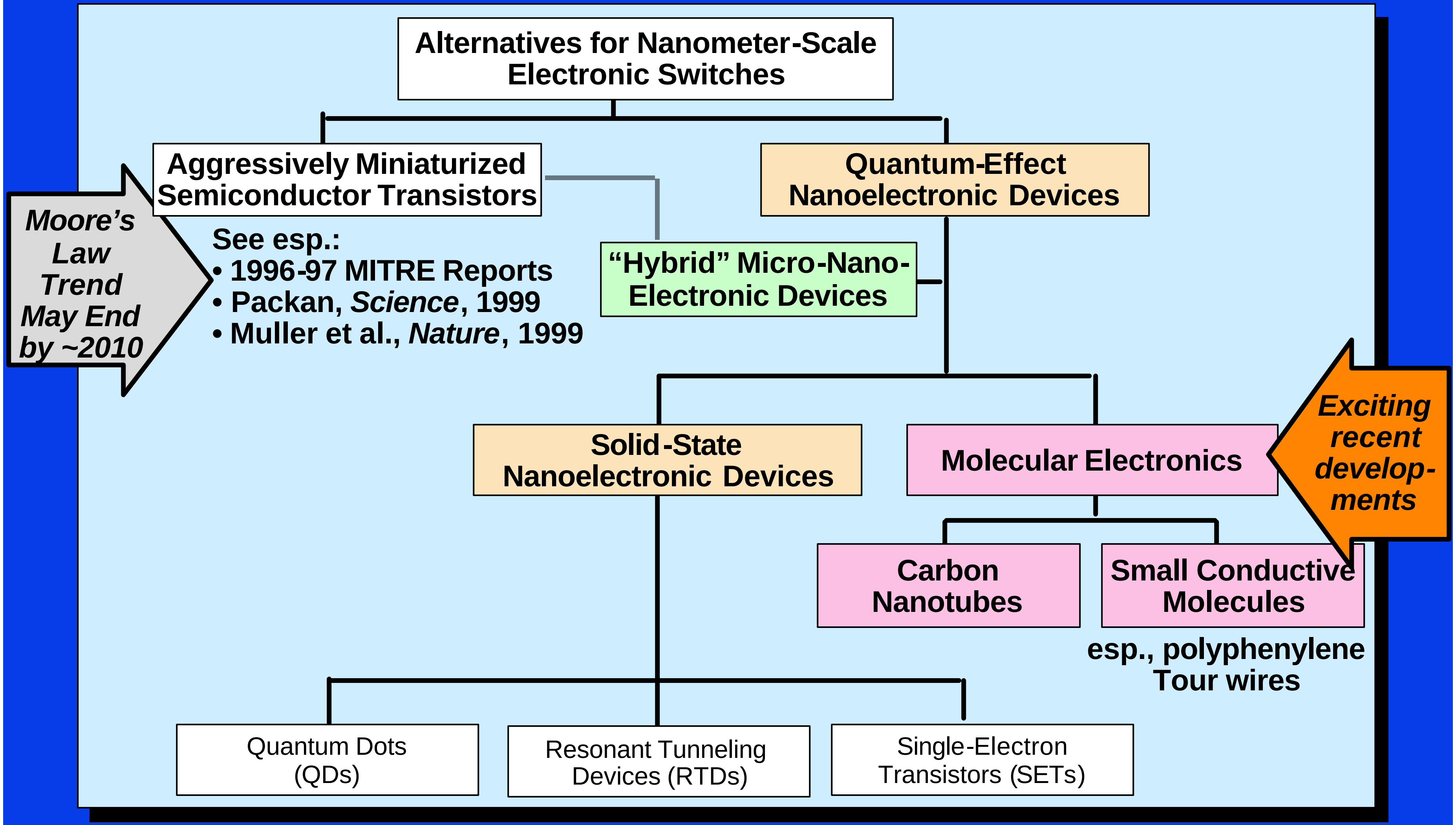
MITRE

Overview and Outline of This Presentation

- **Basis and Introduction**
- **Summary of Main Points**
- **Overview of Nanoscale Device Options**
- **Rationale: Why Molecular Scale Devices**
- **Gallery: Nanoscale/Molecular-Scale Device Options**
  - **FETs**
  - **Carbon Nanotubes**
  - **Hybrid Devices**
  - **Small Molecular Wires & Switches**
  - **Molecular Circuits & Functions**
- **Device Scaling Projection and Comparison**
- **Molecular CAD Development Efforts at MITRE**
- **CAD and Modeling Challenges for Gigascale Integration**
- **Appendix: Solid-State & Molecular Device Challenges**

MITRE

Approaches to Nanometer-Scale Switches: "Overview of Nanoelectronic Devices"*



Alternatives for Nanometer-Scale Electronic Switches

Aggressively Miniaturized Semiconductor Transistors

Moore's Law Trend May End by ~2010

See esp.:

- **1996-97 MITRE Reports**
- **Packan, *Science*, 1999**
- **Muller et al., *Nature*, 1999**

"Hybrid" Micro-Nano-Electronic Devices

Quantum-Effect Nanoelectronic Devices

Solid-State Nanoelectronic Devices

Molecular Electronics

Exciting recent develop-ments

Carbon Nanotubes

Small Conductive Molecules

esp., polyphenylene Tour wires

Quantum Dots (QDs)

Resonant Tunneling Devices (RTDs)

Single-Electron Transistors (SETs)

*** Title of MITRE-written paper that appeared in April 1997 issue of the *Proceedings of IEEE*, which is dedicated entirely to nanoelectronics.**

MITRE

Rationale:
Why Molecular-Scale Devices

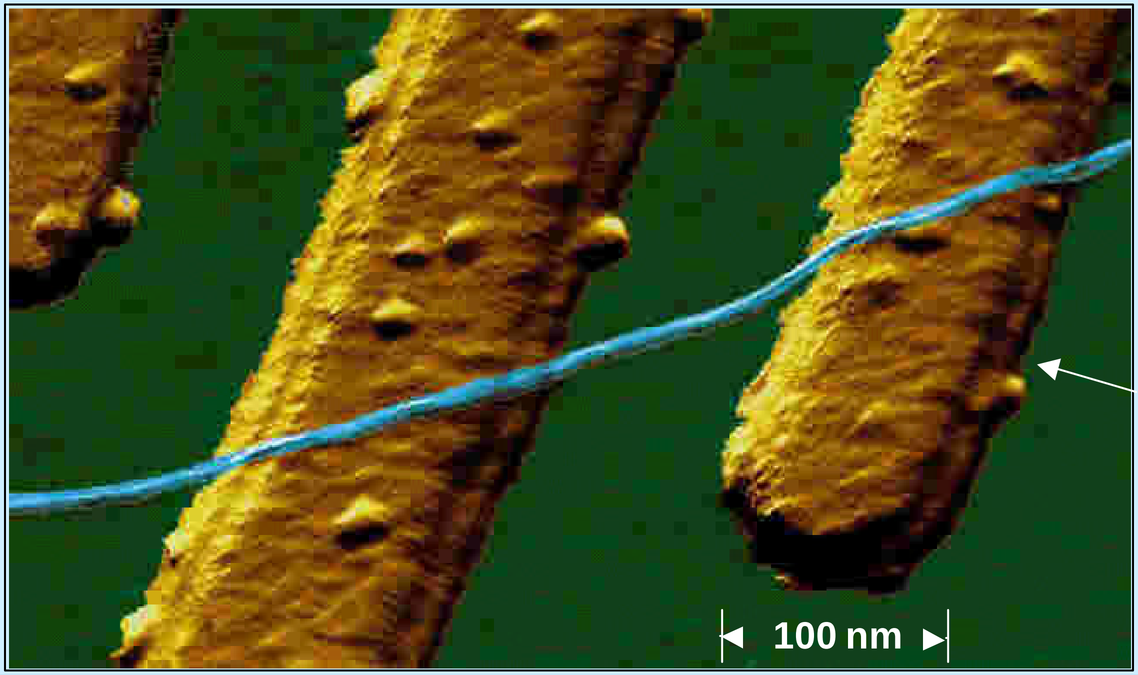
- **Because we're headed there:**
  Planned FETs with ~35 nm features would be close to molecular-scale devices
- **Because we can:**
  True molecular-scale switches & wires already have been demonstrated and are being refined--circuits on the way
- **Because conductive molecules have intrinsic advantages:**
  Small size, great uniformity, ease of fabrication, lower cost --*natural nanometer-scale structures*
- **Because molecules may be able to supplement FETs**
  Hybrid FET-molecular devices may add new circuit and system options--enhanced dynamic and materials properties
- **Because molecules may fill niches that FETs cannot**
  Ultra-high densities, small spaces, and multiple layers (3-D)

FETs = Field Effect Transistors
(i.e., solid-state, bulk-effect microelectronic devices)

MITRE

Molecular Electronic Devices Already Have Been Demonstrated--One Example

- **Buckytubes are very conductive carbon-based molecules**
- **Can carry current over very long distances considered on the molecular scale (~100 microns)**
- **Buckytubes have been interfaced with nanofabricated metal & silicon contacts to make wires and switches**

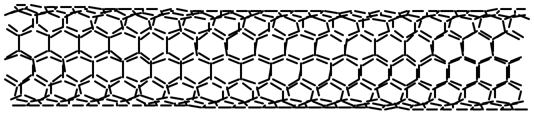


NOTE: **Graphic extracted from the work of S. Tans and C. Dekker, TU Delft, The Netherlands. Published in Nature, 1997.**

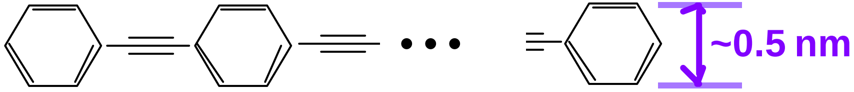
MITRE

Approximate Current Densities for Some Molecular Electronic Devices

Carbon Nanotube Wire



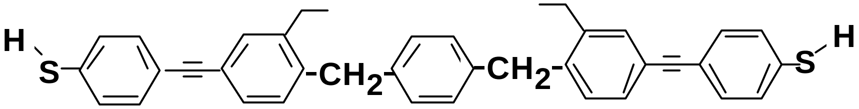
Polyphenylene "Tour" Wire



Molecules can carry enormous current densities

Device	Current Amperes	Current Electrons/Sec	Cross-Sectional Area	Current Density Electrons/nm²–Sec
Polyphenylene RTD	~1 X 10^{-14} amp (~10 picoamp)	9 X 10^{4}	~0.05 nm^{2} (~0.5nm X 0.1 nm)	~2 X 10^{6}
Polyphenylene Wire	3 X 10^{-8} amp (~1 nanoamp)	2 X 10^{11}	~0.05 nm^{2} (~0.5nm X 0.1 nm)	~4 X 10^{12}
Buckytube Wire	1 X 10^{-7} amp (~1 microamp)	6.2 X 10^{11}	~3.1 nm^{2} (radius» 1 nm)	~2 X 10^{11}
Copper Wire	~1 amp	6.2 X 10^{18}	~3.1 mm^{2} (radius» 1 mm)	~2 X 10^{6}

4 nm-long Molecular RTD Switch



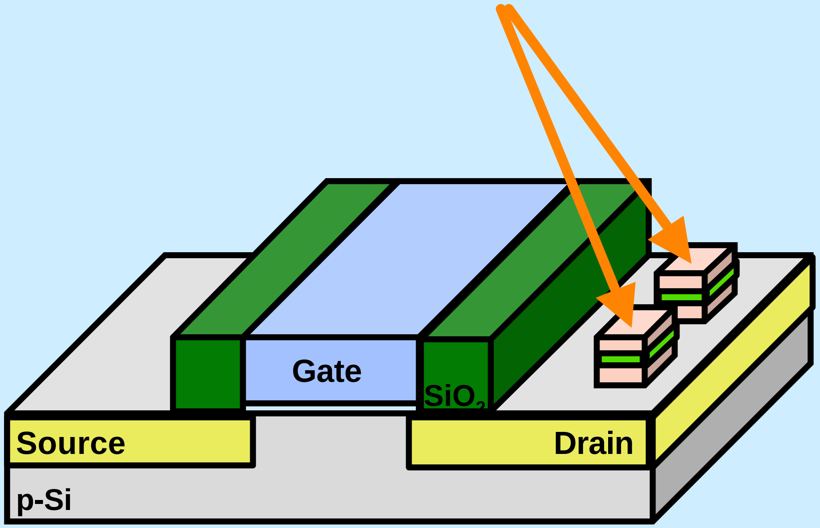
Note: Exp'tal current measurements for polyphenylenes due to Group of Reed at Yale U.;
Current measurements for buckytube due to Dekker's group at TU Delft

MITRE

“Hybrid” Micro-Nanoelectronic Devices May Include Solid-State or Molecular RTDs

FET Enhanced with Solid-State RTDs

Resonant Tunneling Diodes (RTDs) built into drain of Silicon microelectronic transistor

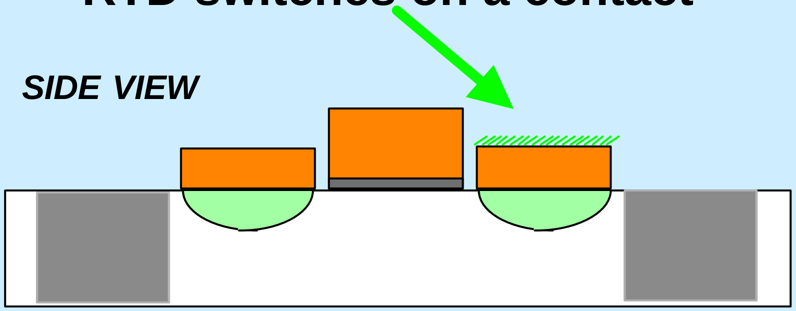


Increases no. of logic states and logic density for microelectronic devices

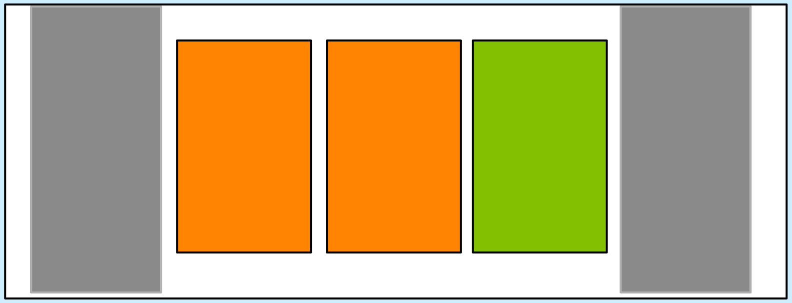
FET Enhanced with Molecular RTDs

Performance of microelectronic transistor might be enhanced by a monolayer of molecular RTD switches on a contact

SIDE VIEW



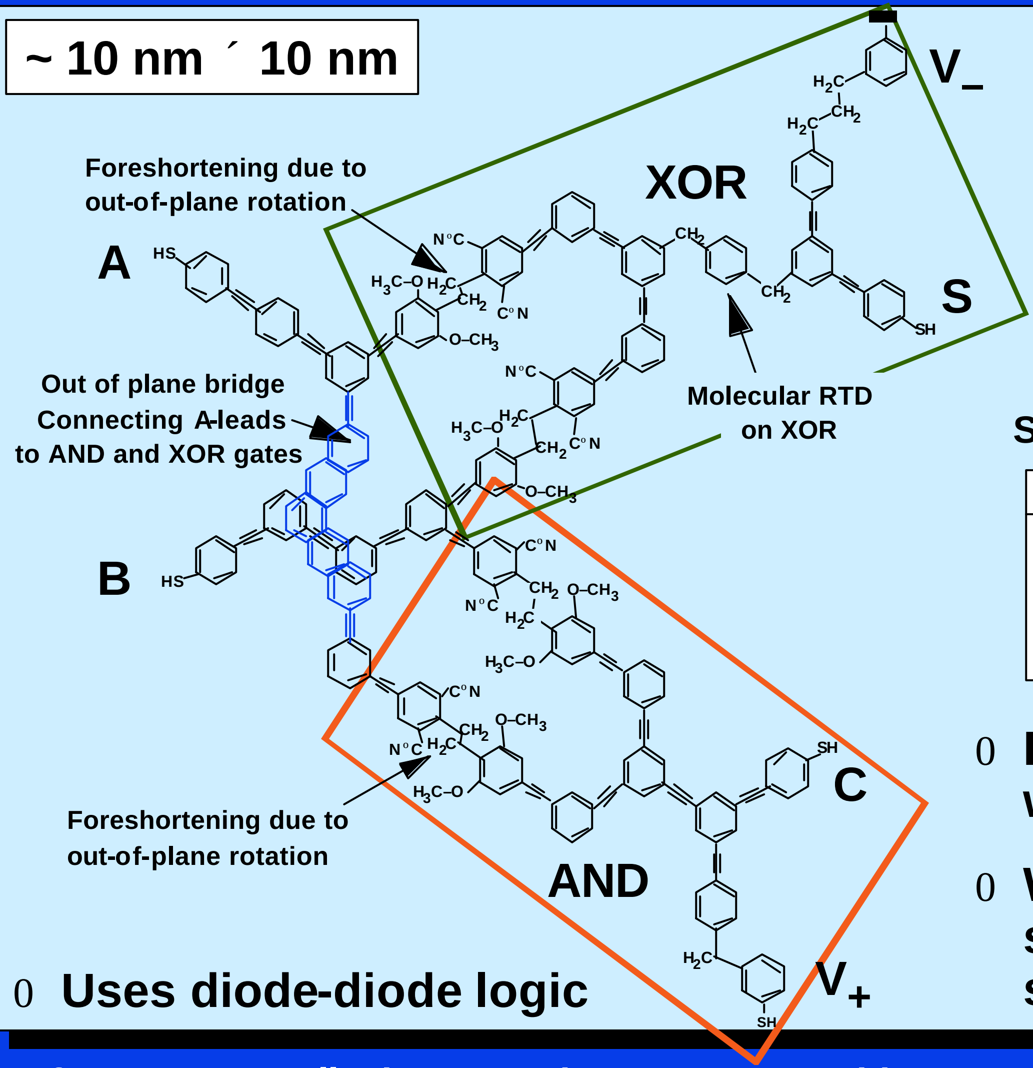
TOP VIEW

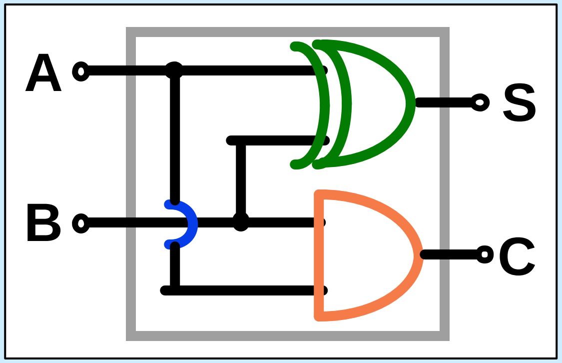


FET = Field Effect Transistor (bulk-effect microelectronic device)
RTD = Resonant Tunneling Diode (quantum-effect nanoelectronic device)

MITRE

Design for a “Pure” Molecular Circuits: Molecular Electronic Half Adder





Sum (S) = XOR

A	B	S
0	0	0
1	0	1
0	1	1
1	1	0

Carry (C) = AND

A	B	C
0	0	0
1	0	0
0	1	0
1	1	1

- **Based upon <u>demonstrated</u> wires and switches**
- **Would be <u>1 million times</u> smaller than comparable silicon micro-circuit**

- **Uses diode-diode logic**

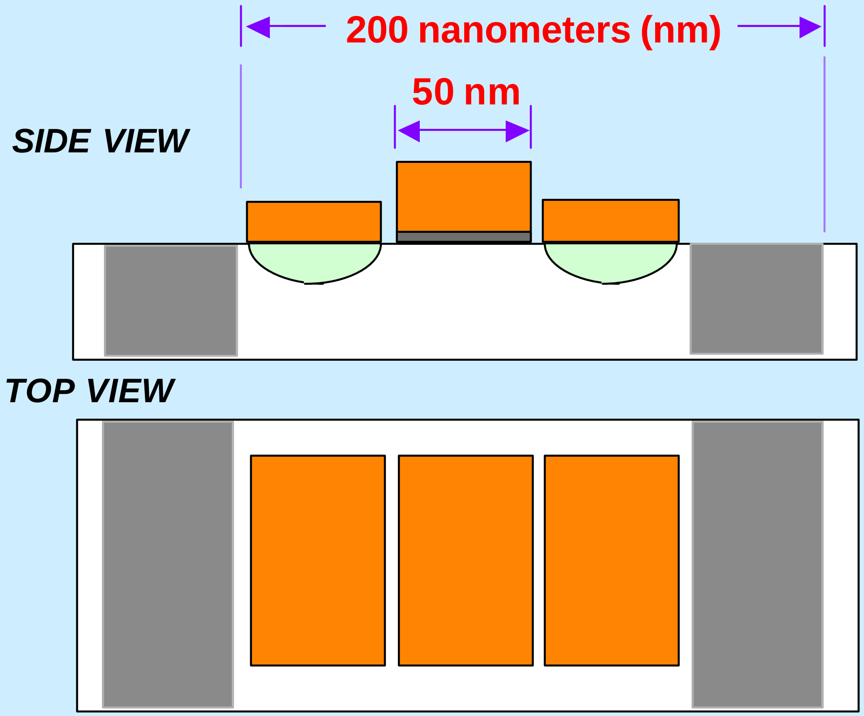
Reference: J.C. Ellenbogen and J. C. Love, “Architectures for Molecular Electronic Computers. 1,” *Proc. IEEE*, March 2000, pp. 386-426.

MITRE

Future Molecular Electronics: Outpacing the Semiconductor Industry Roadmap

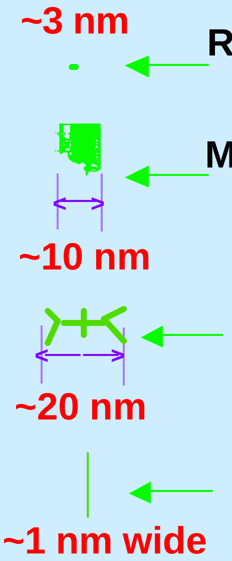
Transistor in 2011 or 2012 ??

Projected by 1997-98 SIA Roadmap, *if* scaling can continue



Before 2010

Beyond the Roadmap



Reed-Tour Molecular Switch (Demonstrated in 1997)

MITRE Molecular Electronic Adder (Proposed for ~2003)

MITRE Nanotube Adder (Proposed for ~2010)

H-P/UCLA Atom Wire (Demonstrated in 1999)

Potential: A simple molecular computer where the Roadmap would place only one switch

Memory Chips	256 Gigabit	>10 Terabit Memory Chip*
CPUs	180 M devices/cm^2	*PC on a grain of salt*

* Based on only 2-dimensional tiling of devices;
Note also: SIA = Semiconductor Industry Association

Overview and Outline of This Presentation

0 **Basis and Introduction**

0 **Summary of Main Points**

0 **Overview of Nanoscale Device Options**

0 **Rationale: Why Molecular Scale Devices**

0 **Gallery: Nanoscale/Molecular-Scale Device Options**
  - **FETs**
  - **Carbon Nanotubes**
  - **Hybrid Devices**
  - **Small Molecular Wires & Switches**
  - **Molecular Circuits & Functions**

0 **Scaling Projection and Comparison**

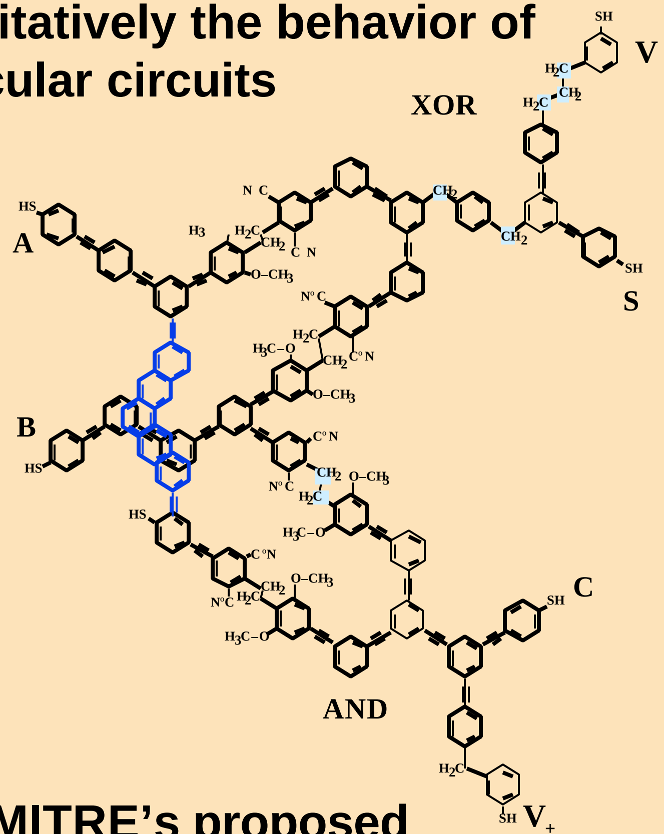
0 **Molecular CAD Development Efforts at MITRE**

0 **CAD and Modeling Challenges for Gigascale Integration**

0 **Appendix: Solid-State & Molecular Device Challenges**

MITRE's Research and Development In Support of DARPA Moletronics Program

Require software tool to predict quantitatively the behavior of molecular circuits



...like MITRE's proposed molecular electronic half-adder

DARPA-Sponsored Task:

Prototype molecular circuit design software tool--"MolSPICE"

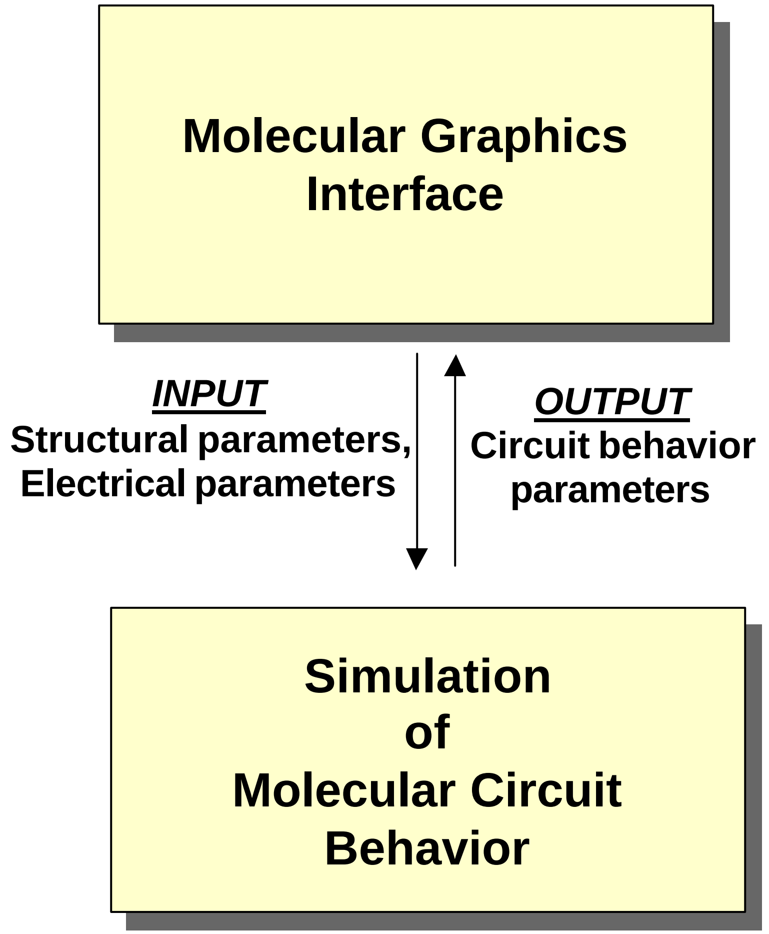
Research and Development for Molecular Circuit Design Tool (“MolSPICE”)

Notable Features of CAD Tool

0 **Graphics Interface:**
Operates via Web browser

0 **Molecular Circuit Simulation**

- ***Must both account for quantum mechanics and operate rapidly***
- **Two strategies**
  - = **Introduce approx. quantum coupling**
    w/ perturbation theory and parametric device models
  - = **Aggregate quantum effects into approximate equations that govern *entire circuits*; then assemble functions from circuit modules**



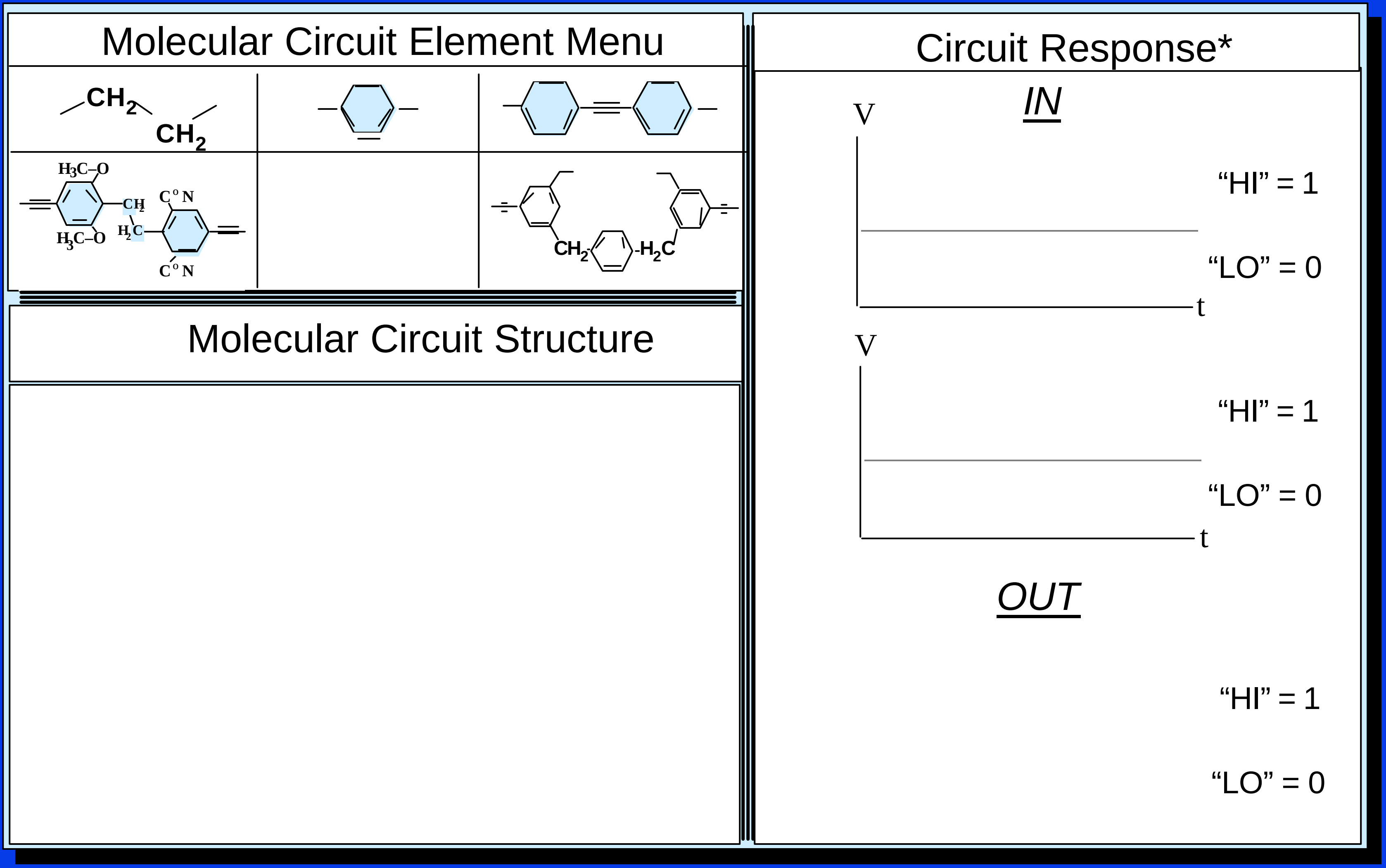
Molecular Graphics Interface

INPUT
Structural parameters,
Electrical parameters

OUTPUT
Circuit behavior
parameters

Simulation of Molecular Circuit Behavior

Appearance of MolSPICE
Molecular Circuit Design Tool Interface



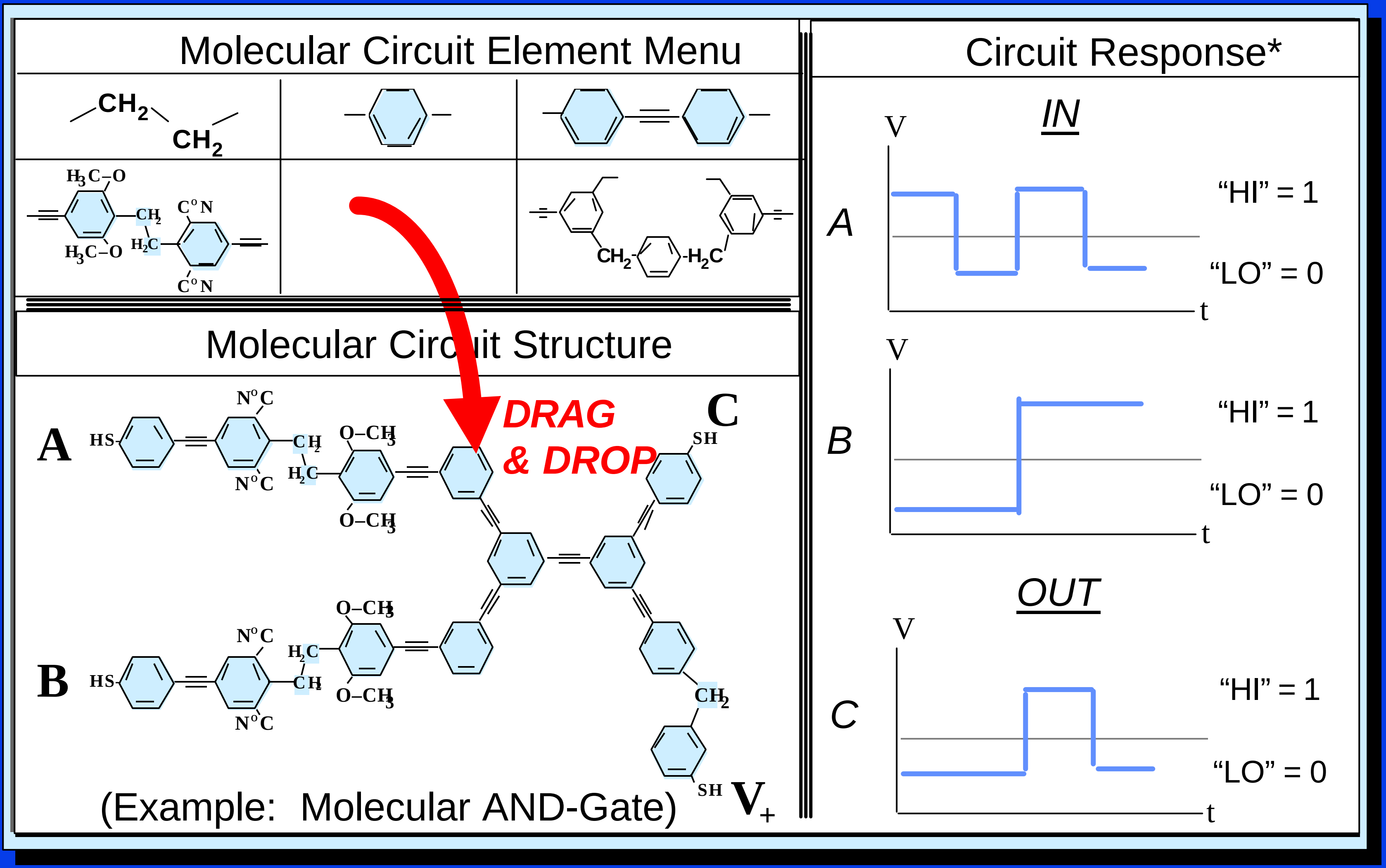
Molecular Circuit Element Menu

Molecular Circuit Structure

Circuit Response*

*** NOTE: Graphs shown here plot voltage (V) vs. time (t); other response measures also will be employed**

Envisioned Operation of MolSPICE Molecular Circuit Design Tool



*** NOTE: Graphs shown here plot voltage (V) vs. time (t); other response measures also will be employed**

MITRE

CAD/Modeling Challenges for Gigascale Integration

- Vertical integration of models at different levels
  - Materials & doping
  - Quantum Effect Devices
  - FETs
  - Circuits
  - System architectures--incl. interconnect & thermodynamic considerations, as well as processor parallelism, etc.
- Rapidly calculating quantum effects in circuit-level aggregations of devices *and* taking advantage of them
- Accounting for:
  - Error and fault tolerance in ultra-dense systems involving local quantum effects, plus device-device quantum couplings
  - Enormous numbers of devices and small circuits
    - 10 nm x 10 nm footprint --> 10^10 devices/mm^2
    - 100 nm x 100 nm footprint --> 10^8 devices/mm^2
  - Multi-state and multi-function devices
  - Multiple *types* of devices in “hybrid” switches and circuits involving quantum effect switches, as well as FETs

MITRE

CAD/Modeling Challenges for Gigascale Integration (Concluded)

- **Possible necessity of modeling ultra-dense 3-D circuits and architectures**
- **Making use of enormous number of circuits that can be squeezed into such small areas and/or volumes--massive parallelism on a “chip”**
- **User interface and coherent representation of coupled problems on a range of scales**
- **Web-based architectures and operation for software, including databases and user interfaces (browser-based)**

~Appendix: Device Challenges for Gigascale integration~

Device Challenges for Aggressively

From Goldhaber-Gordon *et al.*, 1997

- **Avalanche breakdown due to high electric fields over very short distances--device damage**
- **High heat dissipation--esp. from gate switching**
- **Vanishing bulk properties and nonuniformity of doping**
- **Shrinkage of depletion regions--source-drain leakage**
- **Shrinkage and unevenness of gate oxide--gate-channel leakage--*tunneling***
- **Quantum effects**

From Packan, 1999

- **Dopant solubility in Si--may not be sufficient to continue to maintain low resistances**
- **High electric fields cause breakdown of thinner oxide layers required for shorter devices**
- **Current leakage through thinner gate oxide due to quantum effects**
- **Uneven distribution of dopant atoms**

From Muller *et al.*, 1999

- **Uneveness and thinning of gate oxide may be a limit to scaling**

Device Challenges for Solid-State Quantum Effect Switches

- Need for very small size of “islands,” barriers, and quantum wells to ensure effective high T operation
- Stringent requirements for device uniformity--a few atomic diameters for metal and semiconductor components
- Charge trapping
- Lack of a satisfactory oxide or other readily usable insulating material (to act as analog to SiO_2 in Si devices)
- Issues with “manufacturability” of III-V semiconductors (Ga-As, etc.)
- Difficulty of achieving satisfactory heterojunctions in Group IV (Si, Ge, etc.)

Device Challenges for Molecular Quantum Effect Switches

- **Switch fabrication**
- **Refinement of**
  - **Intramolecular doping and strategies**
  - **Internal quantum barriers**
  - **Molecular “alligator clips” and electrical contacts**
- **Improved understanding & models of observed molecular conductance and molecular switching mechanisms**
- **Molecular 3-terminal devices with gain**
- **Satisfying simultaneously the competing requirements of speed, low power/low dissipation, and sufficient noise margins (one may have to be sacrificed)**

MITRE

Primary Architectural Issues for Molecular-Scale Electronics

- **How to design logic gates, functions, extended circuitry using molecules**
- **Making reliable, uniform electrical contacts with molecules**
- **Current based: high resistance of narrow molecular wires(?); Charge based: trapping in meta-stable states**
- **Interconnect issues: Geometric & Dynamic (slowdown in small interconnects)**
- **Assembly strategies for extended systems of smaller molecular logic units--arranging and organizing molecules**
- **Achieving gain**
  - **Gain/amplification is *essential* in extended logic**
  - **Primarily 2-terminal molecular electronic devices <u>without</u> gain have been demonstrated, thus far**
- **Fault tolerance: Strategies for *mitigating* effects of errors**
- **Dissipation: Cooling of extended ultra-dense circuitry or charge receptacles/cells**

CAD Challenges for Advanced Device Integration

Daniel J. Radack

Microsystems Technology Office

CAD Workshop

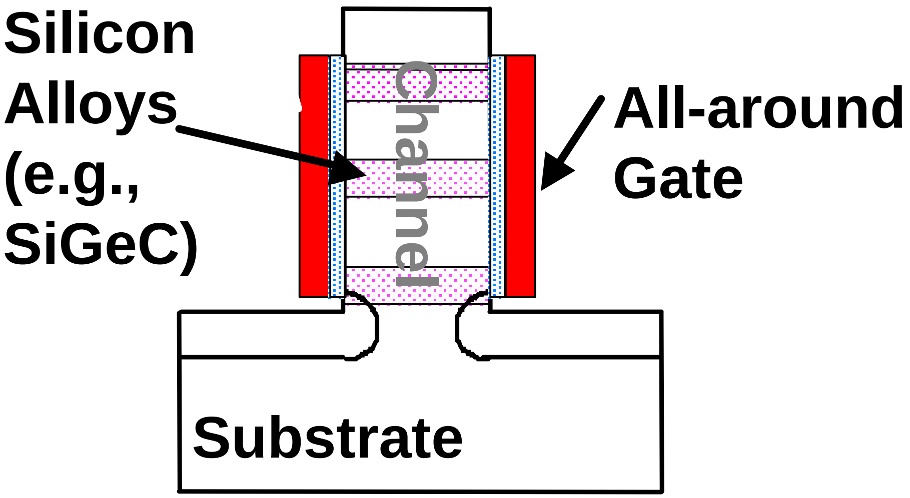
CAD for Device Integration

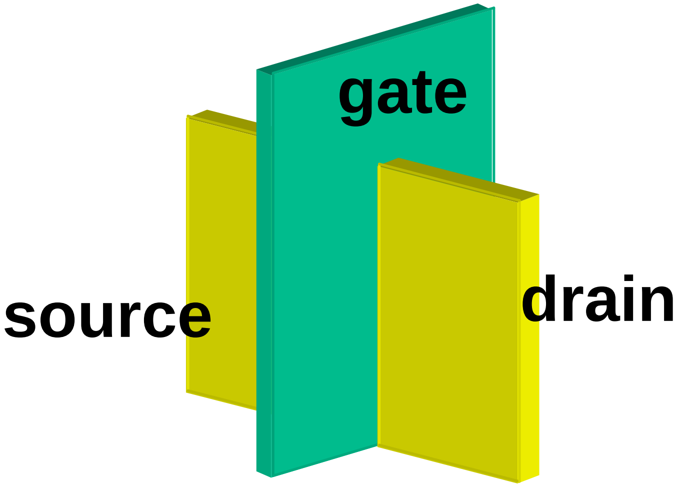
- Devices
  - Non-planar structures, nano-sized structures, contacts
  - Molecules, qubits, quantum and classical
  - 3-D Integration
- Interconnects
  - Planning/routing, scaling laws less clear than devices and more layers for trade-offs
  - Signals on small wires, power, clock
  - Seamless incorporation of new technologies
- Power
  - Delivery and dissipation (100-1kW/cm^2)
- Coupled design and fab
  - Worst/best case corners not good enough
- CAD Efficiency
  - 25 person group max’s at 1M transistors, teams <100 people for practical purposes
  - HW/SW interactions and co-design

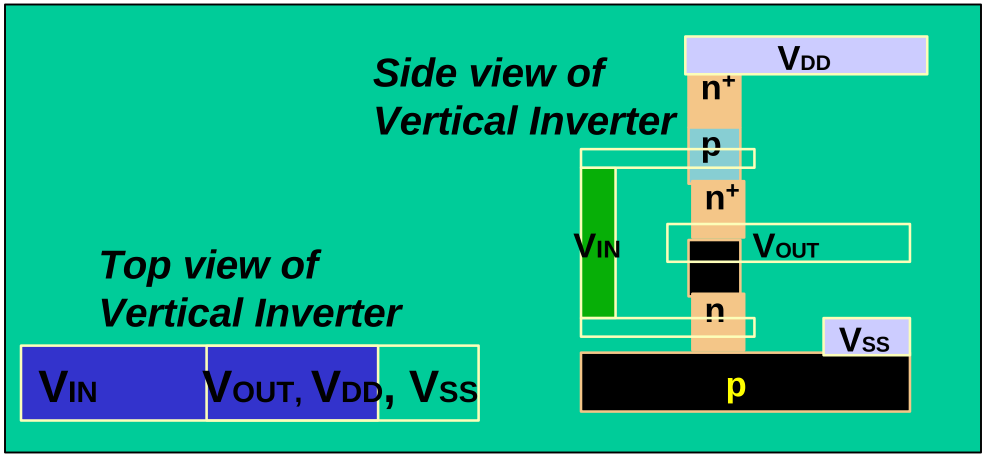
Power Dissipation

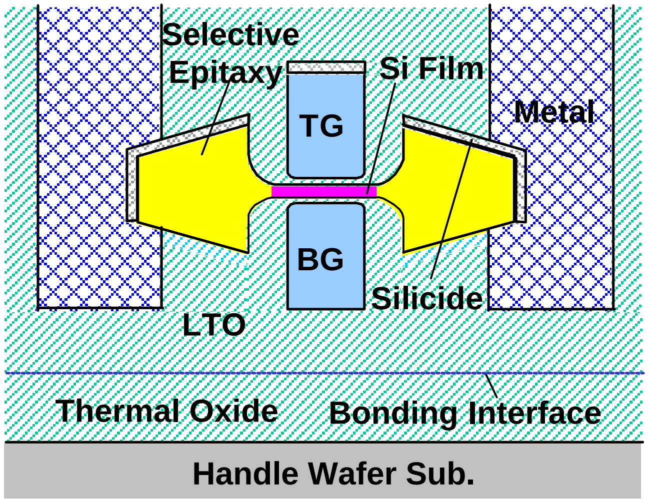
- More than calculation of CV^2f
- Interconnects and I/O drivers
- Analog, RF, mixed signals
- Optical I/O conversion efficiency (e-/photons), clock distribution
- Embedded power management hardware
- Software, switching activity

Non-planar Devices



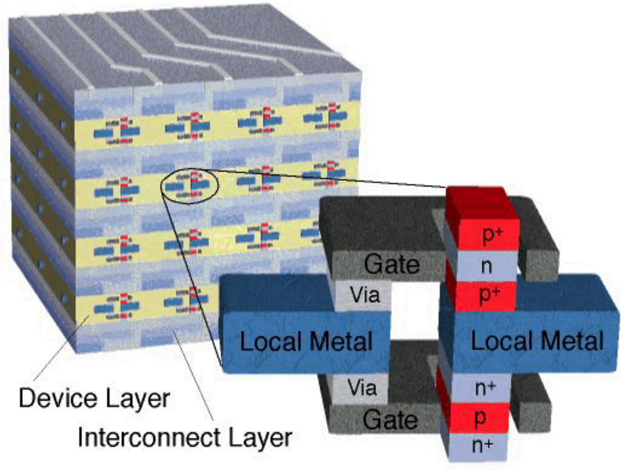






Signals, power, ground for billions of nanosized 3-D devices

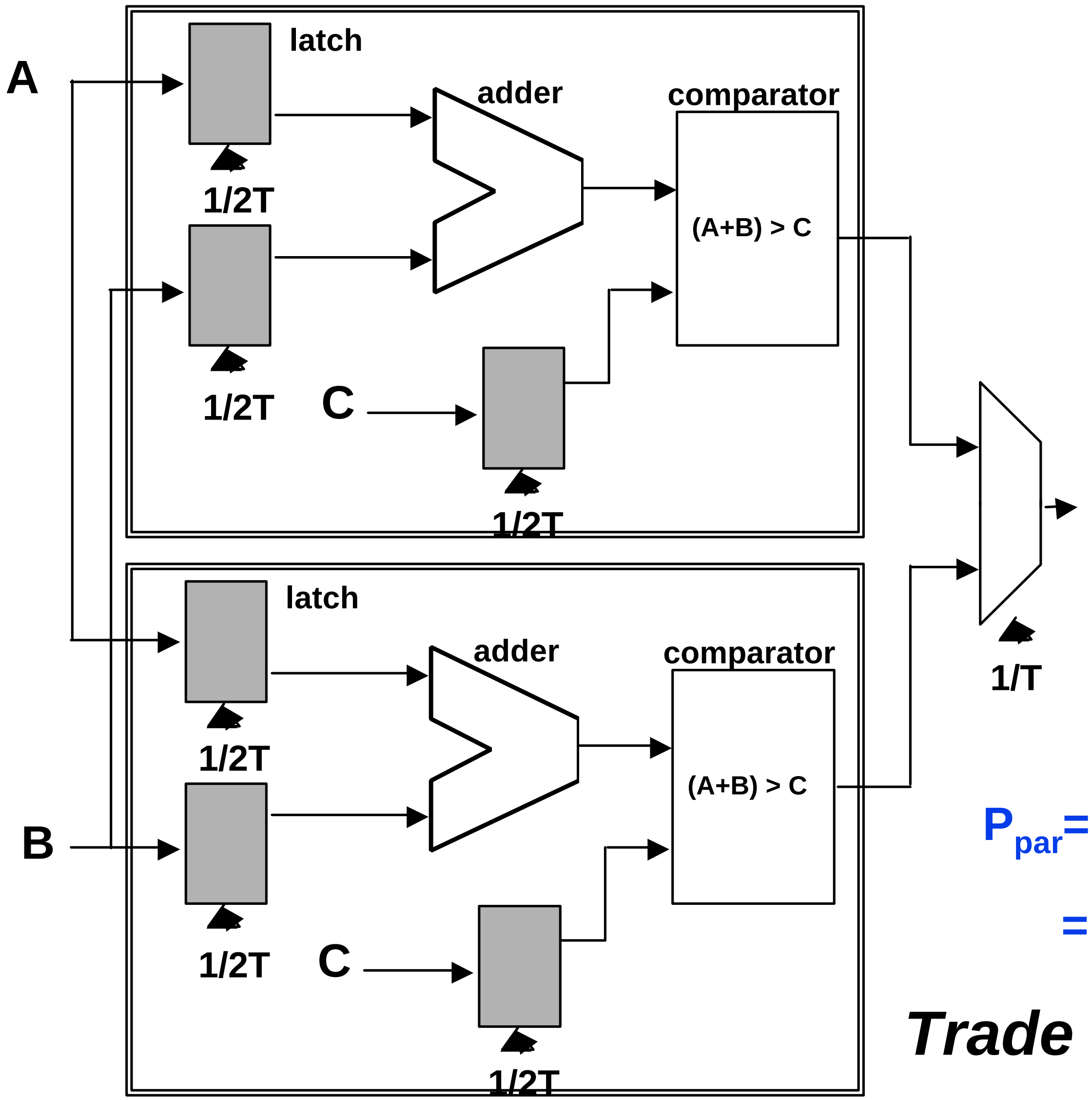
3D Integration



Thermal Issues

- Complex issue, highly dependent on circuit architecture, function, and composition
- CMOS scaling factor ($1/\alpha$), then power also scales by $1/\alpha$, power density does not scale!
- One idea - exploit available transistors to lower power (double area, halve f, decrease V, power reduces by V^2)

Fixed Throughput
Parallel Datapath



- duplicate, parallel datapaths
- half the clock frequency ($f_{par} = 0.5 \; f_{ref}$)
- almost half the drive voltage ($V_{par} = V_{ref} / 1.7$)
- more than doubles chip area & capacitance ($C_{par} = 2.15 \; C_{ref}$)
- same throughput

but power reduced by almost a factor of 3

$$P_{par} = (2.15 \; C_{ref}) \bullet (V_{ref} / 1.7)^2 \, (0.5 \; f_{ref})$$

$$= 0.36 \; P_{ref}$$

Trade Device Count for Power

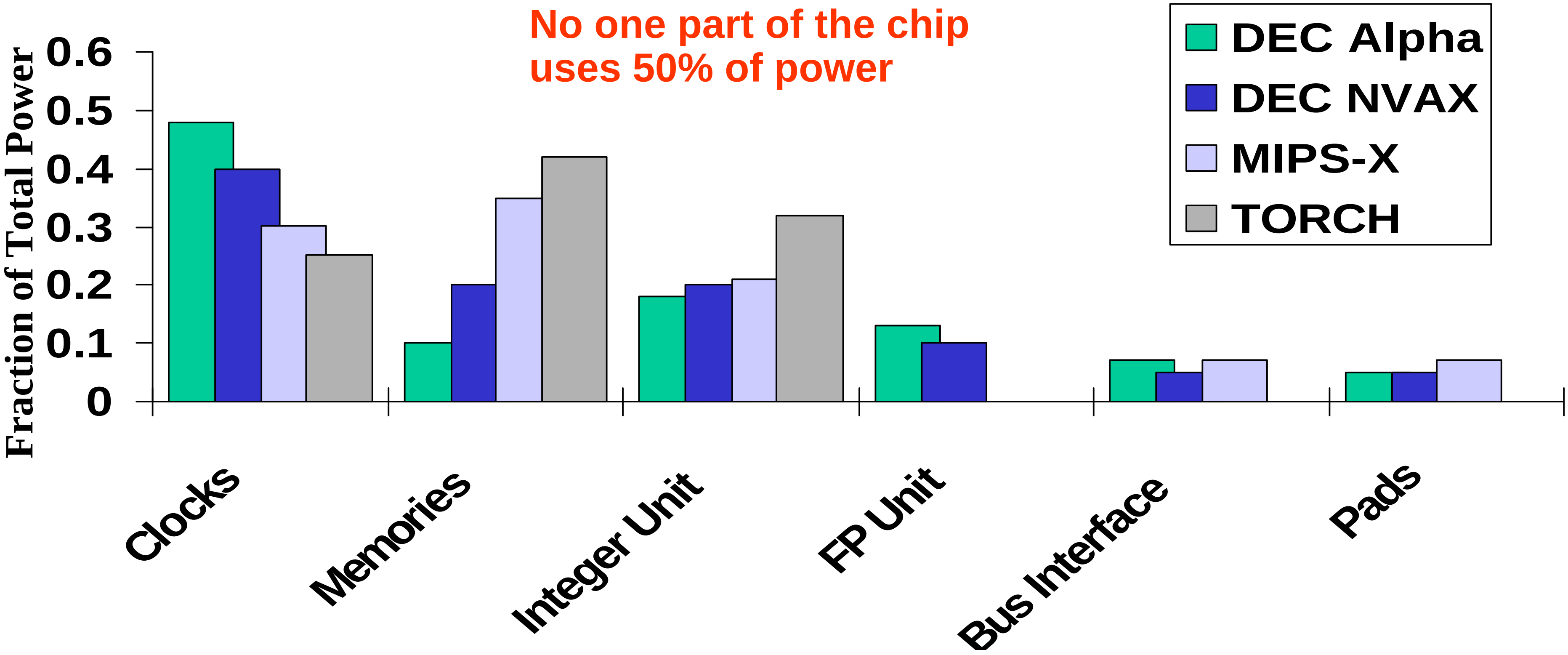
Power Estimation

- **uses final, completed chip description**
- **partition into functional units**
- **switch-level simulator using node capacitances and transition history**

need

Rapid, accurate, fine-grain power estimation tools

integrated cost, performance, and power design tools



Synthesis of Mixed Technology IC’s

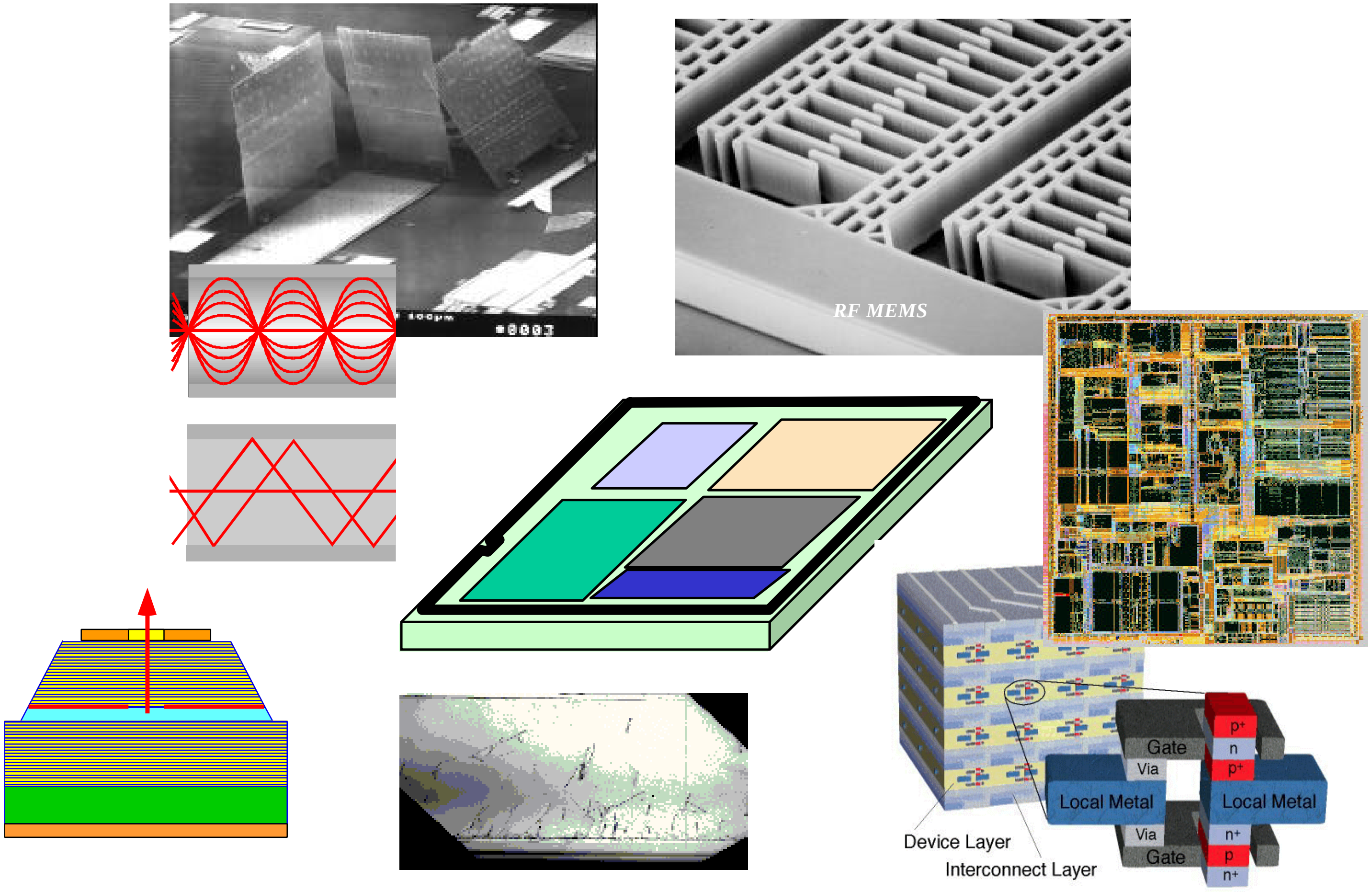
Behavioral Description

To

Lay-out and Recipe

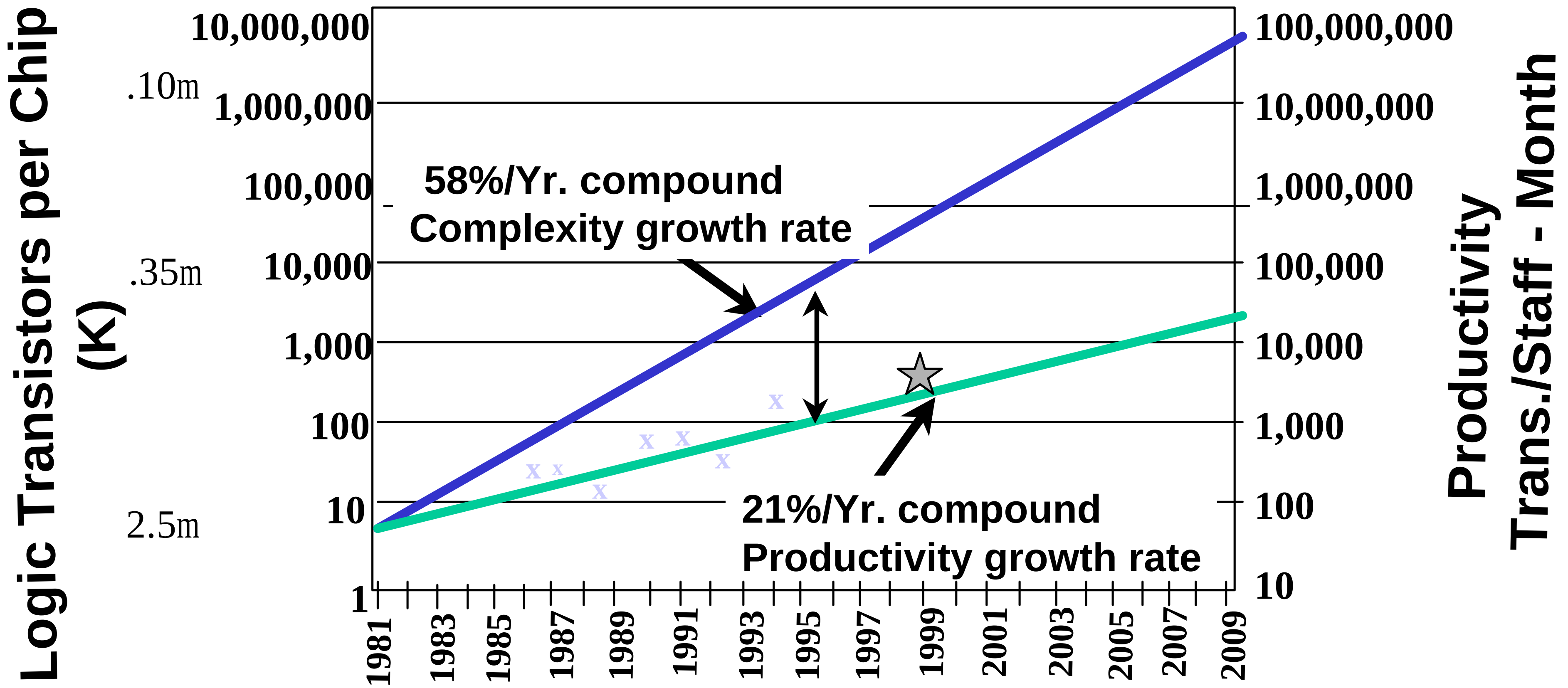
With

Design for High Yield



Have an opportunity to obtain new SoC functionality through incorporation of diverse materials/devices, but need synthesis/integrated CAD.

Design Productivity “Gap”



58%/Yr. compound Complexity growth rate

21%/Yr. compound Productivity growth rate

FCRP addressing rebuilding RTL foundation and component based design

Source: SEMATECH

Suggested Focus

- Tools and models to enable design and fabrication of truly heterogeneous integrated microsystems
- Tools to enable design of 3-D integrated circuits
- Coupled design and fabrication – capturing whatever device physics phenomena that are needed to build circuits
- CAD to figure out how to create and understand new devices

What’s the Problem?

- Current EDA industry focus is [rightly] on support of current generation fabrication
- Scaling of design methodology for next generation, but scale is linear
- Starts breaking in the generation after next, and gets worse near exponentially
- Have an opportunity to obtain new SoC functionality through incorporation of diverse materials/devices, but need synthesis/integrated CAD.
- Need to account for rest of system/software during design phase.

Designing for the Very Many

Don MacMillen

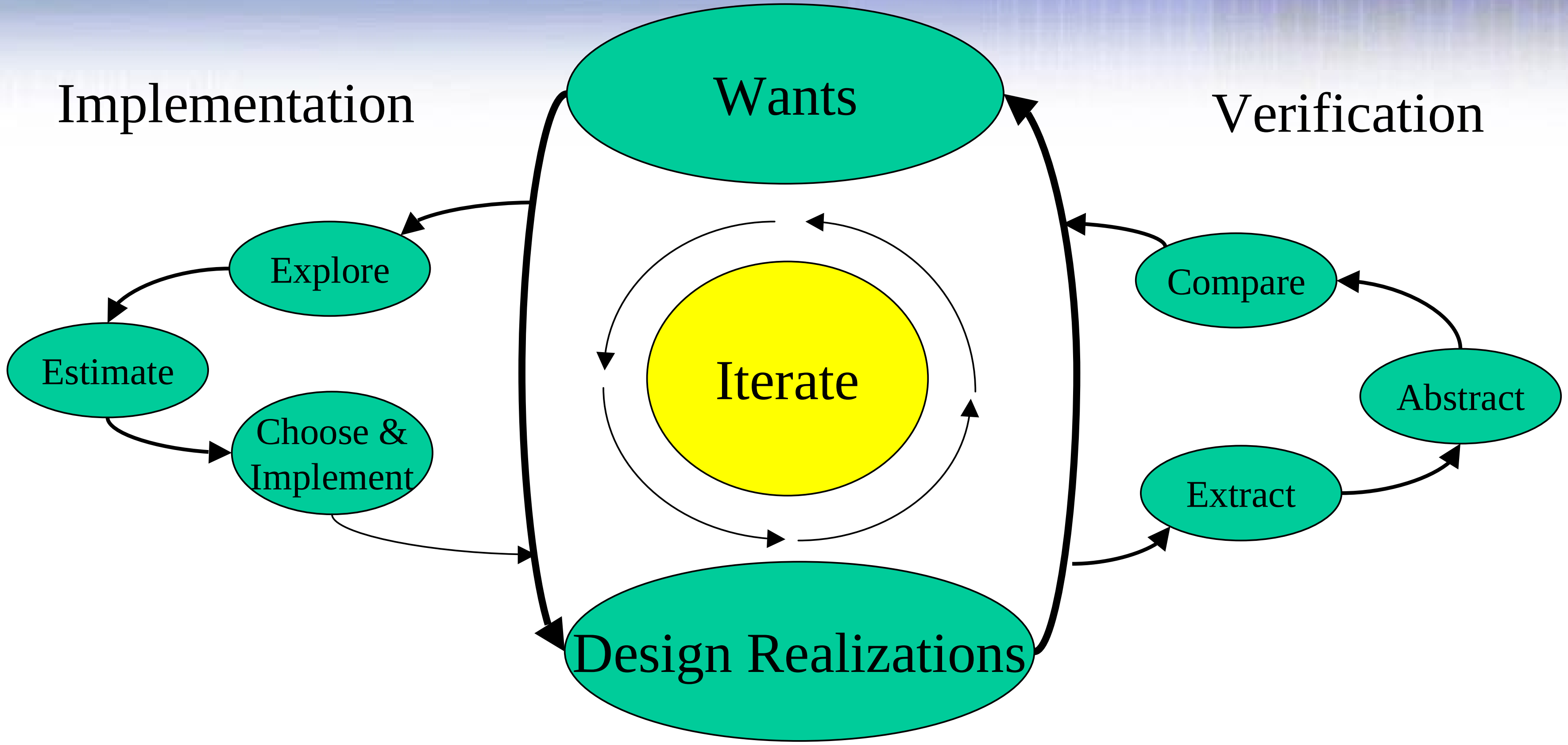
Vice President, Advanced Technology Group

Synopsys

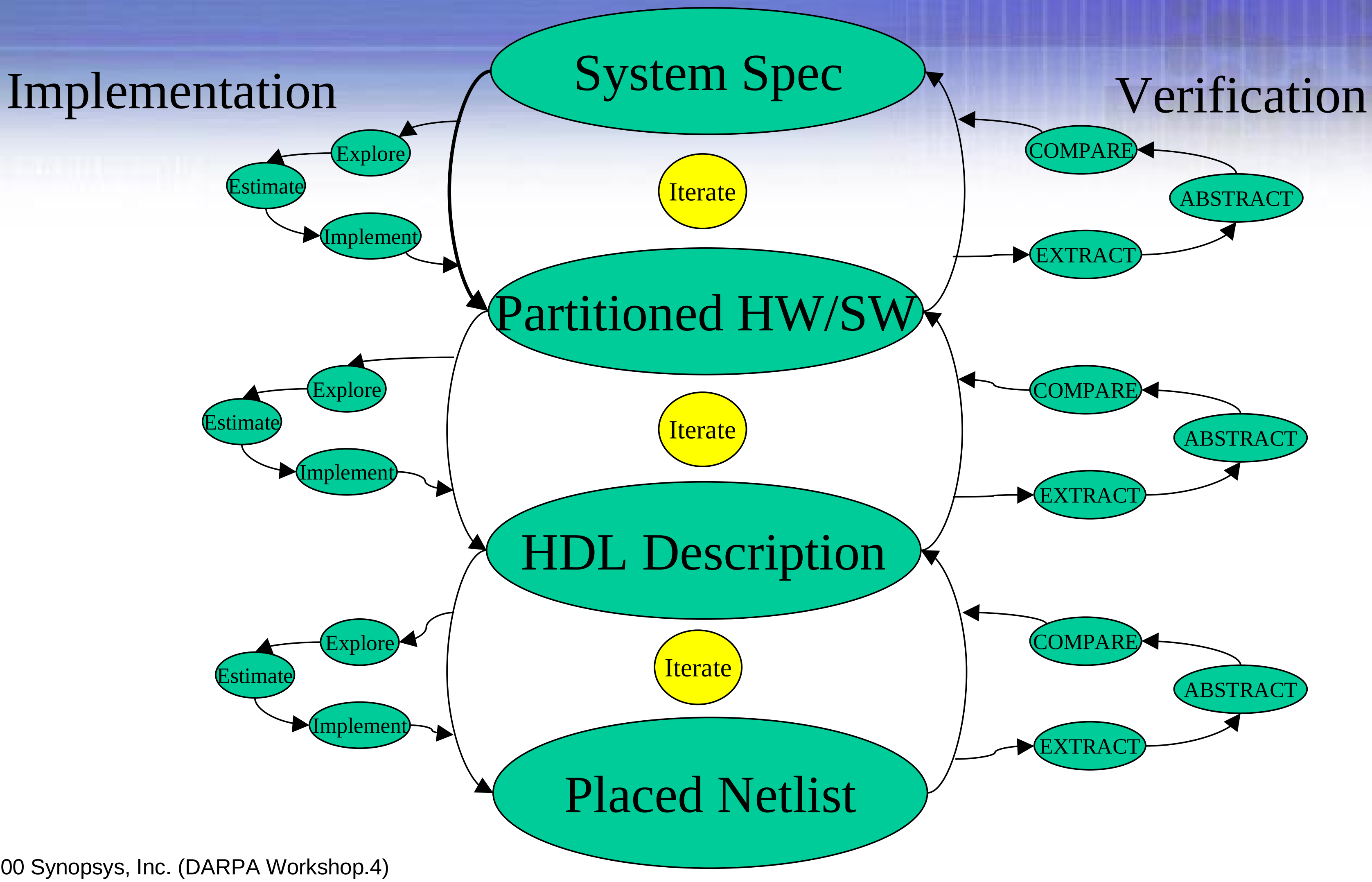
Today’s Design Flow Problems

- **This talk will touch on some of the problems in designing *Large* Systems.**
- **Specifically not looking at problems dealing with *small* or *different* device types.**
- **Today’s immediate problem is *Timing Closure* in the logical / physical domain**
- **One of the reasons that designers are so adamant about solving timing closure is that they cannot afford to iterate earlier into the design cycle.**
- **Why? Because verification is too hard and getting harder.**

The Conceptual Design Flow



The Conceptual Design Flow



Implementation

Verification

System Spec

Explore

Estimate

Implement

Iterate

COMPARE

ABSTRACT

EXTRACT

Partitioned HW/SW

Explore

Estimate

Implement

Iterate

COMPARE

ABSTRACT

EXTRACT

HDL Description

Explore

Estimate

Implement

Iterate

COMPARE

ABSTRACT

EXTRACT

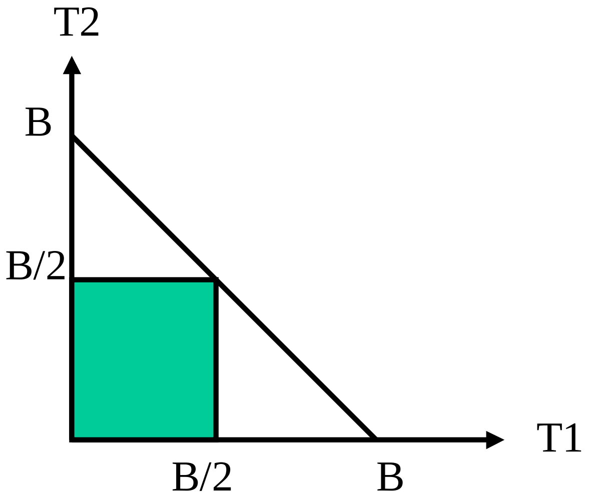
Placed Netlist

HW / SW Performance Estimation

- Software estimation remains difficult because of problems in modeling the environment
  - One approach is to run code on a ISS with “worst” case input set and then heuristically derate the simulated run time
  - Another is to eliminate all non deterministic choices in the program (i.e. data dependent loop bounds) and then solve for max on the control flow graph.
- Hardware estimation usually depends on “fast but accurate” synthesis. This is still problematic today.
- The problem of constraint propagation (a.k.a. design budgeting) will be key in obtaining designs that meet our targets. This is a very difficult problem.

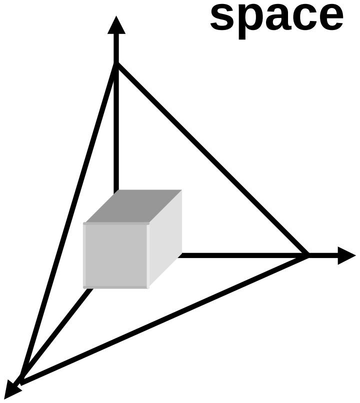
Design Budgeting: a dimensional analysis

- **Assume we wish to distribute a budget B between two blocks.**
  - **We have T1 + T2 < B**
  - **The optimal naïve budget is given by T1 < B/2 and T2 < B/2**
  - **This budget only covers 1/2 of the feasible constraint space**



Design Budgeting: a dimensional analysis

- Now assume we wish to budget three blocks.
  - We have T1 + T2 + T3 < B
  - The optimal naïve budget is given by T1 < B/3,   T2 < B/3 and T3 < B/3
  - This budget only covers 2/9 of the feasible constraint space

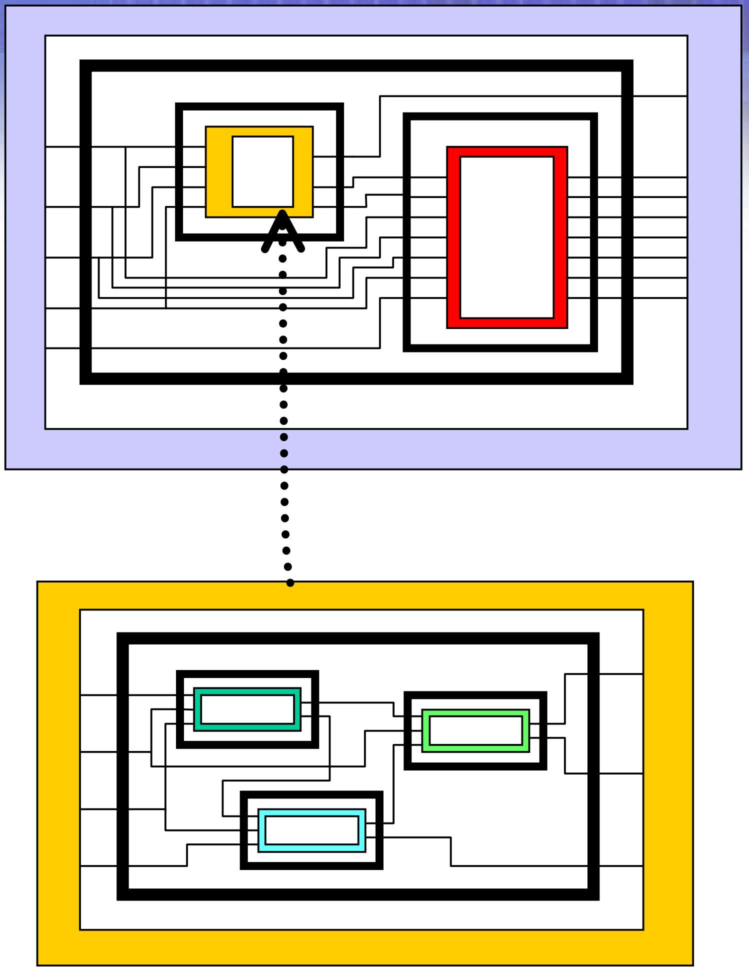


Volume of cube = (B/3)^3 = (B^3)/27
Volume of pyramid = (AH)/3 = (B^3)/6

In n-space:
Volume of cube = (B/n)^n
Volume of pyramid = (B^n)/n!
Only n!/(n^n) of feasible search space is covered

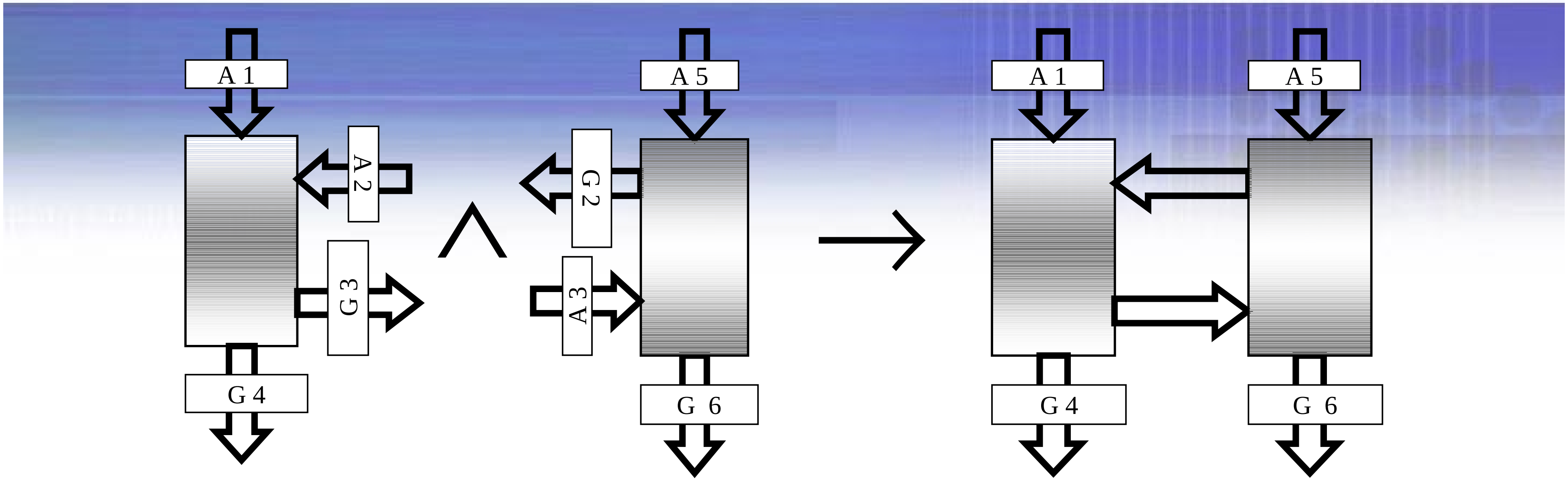
n	n!/(n^n)
1	1
2	0.5
3	0.222
4	0.094
5	0.038
6	0.015
7	0.006
8	0.002

Compositional Verification



- Model checking can't handle full chip implementation details
- Verify high level design using abstract models for components
- Check that components are refinements of abstract models

Assume-Guarantee Reasoning



- **Components correct implies system correct**
  - designer must specify interfaces
    - strong enough as assumptions
    - weak enough as guarantees
  - This task remains incredibly difficult

Can Design Reuse help?

- We still need to verify the system of interacting components meets our needs.
- In an era of SoC’s composed of thousands of IP blocks, what quality level do we need for dependable operation?
- Can we build dependable systems from undependable components?
- Do we build “fault tolerant” SoC’s?
  - How do we define Faults and Failures for SoC’s?
  - Are the concepts of safeness and liveness useful?
  - Is there a reusable “detect and correct” paradigm?

Tools for System Integration Choice

Wojciech Maly
CMU

Agenda

1. System-on-chip is not the only choice we will have;
2. Choice of system integration strategy will be more difficult to make;
3. There exists a need for tools facilitating right choice.

05/5/00

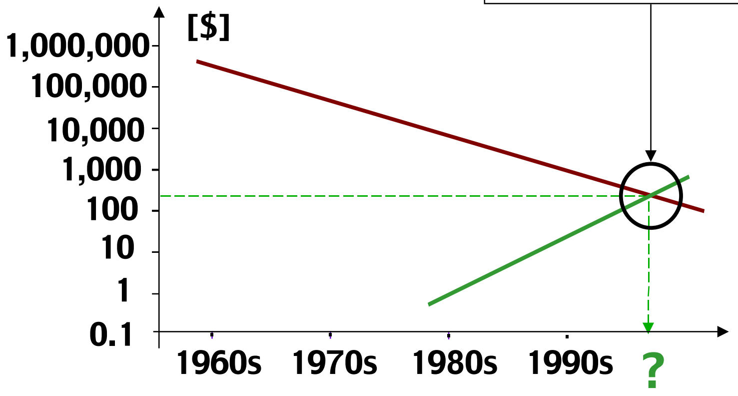
Outline

1. Evolution trends
2. System integration options:
    a. Monolithic
    b. Hybrid
    c. 2.5 D
2. Choice of system integration strategy
3. Needed performance/cost models
    a. Cost case study
    b. Performance case study;
4. List of needed tools

Evolution Trends

Price of the system sold in high volume and cost of a single IC

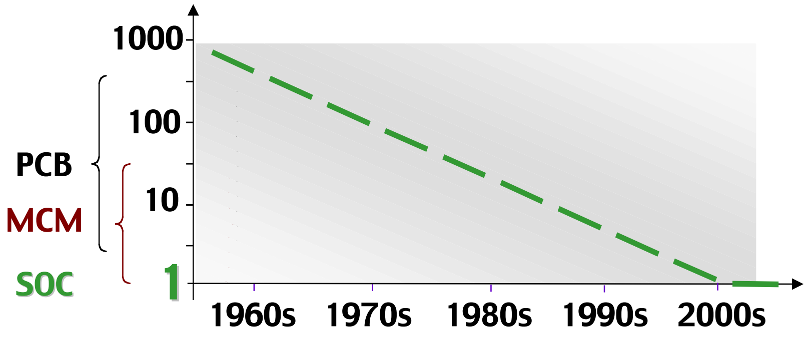
The END of Moore's Law



Evolution Trends

Carnegie Mellon

Number of IC components in systems sold in volume

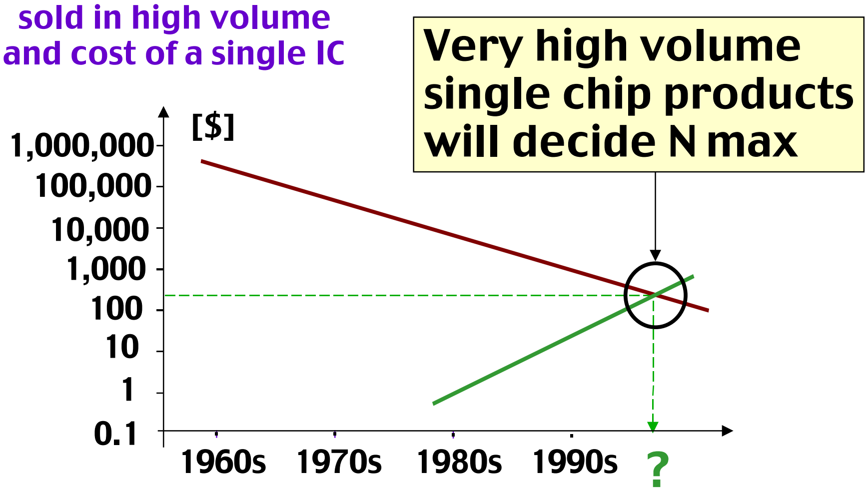


GSRC

Evolution Trends

Carnegie Mellon

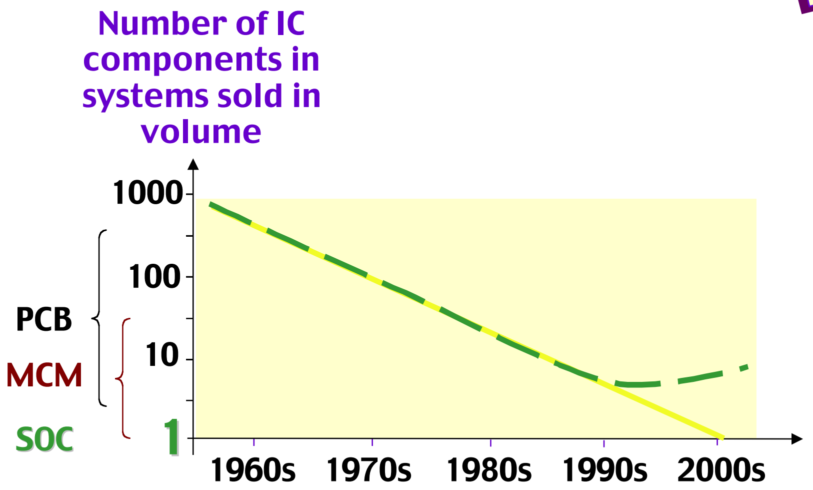
Price of the system sold in high volume and cost of a single IC



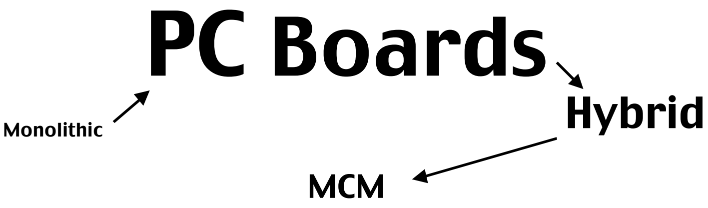
Very high volume single chip products will decide N max

GSRC

Evolution Trends



Evolution Trends



PC Boards

Hybrid

MCM

Monolithic

Evolution Trends

Carnegie Mellon

PC Boards

Monolithic

Hybrid

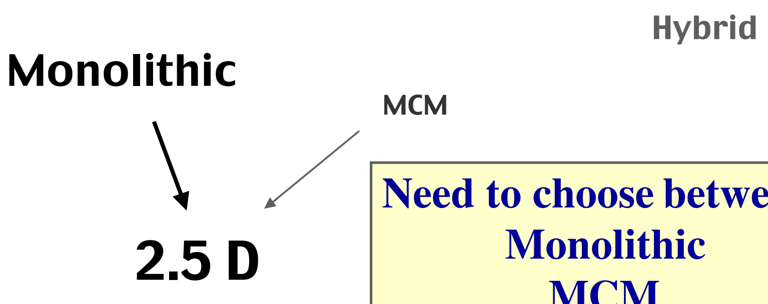
MCM

GSRC

Evolution Trends

Carnegie Mellon

PC Boards



Hybrid

Monolithic

MCM

2.5 D

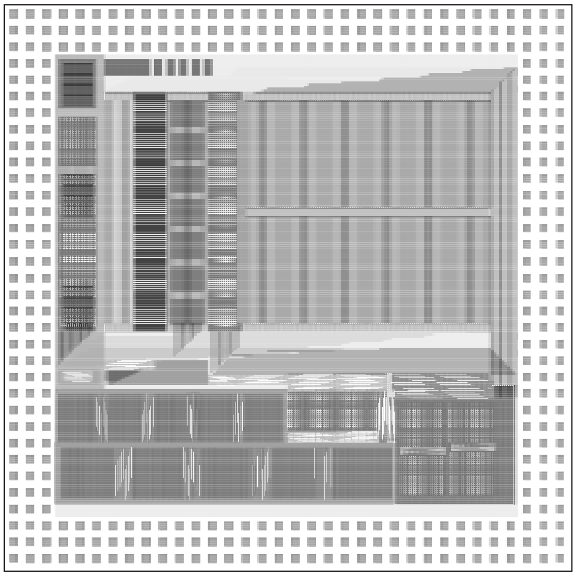
Need to choose between:
Monolithic
MCM
2.5 D

GSRC

Monolithic Integration

Current vision:

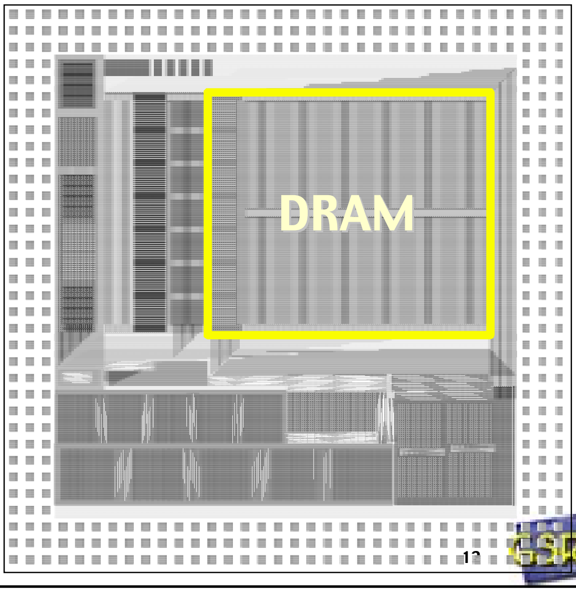
ENTIRE SYSTEM on SINGLE CHIP ! ?

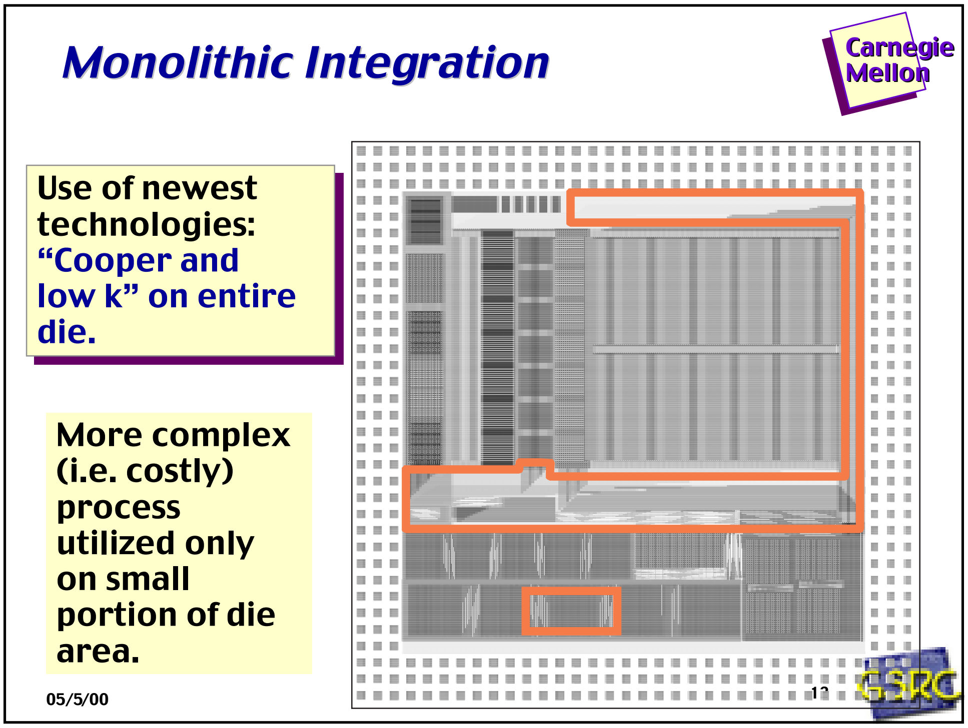


Monolithic Integration

Need for integration of Mixed Technologies: **Embedded Memories**

More complex (i.e. costly) process



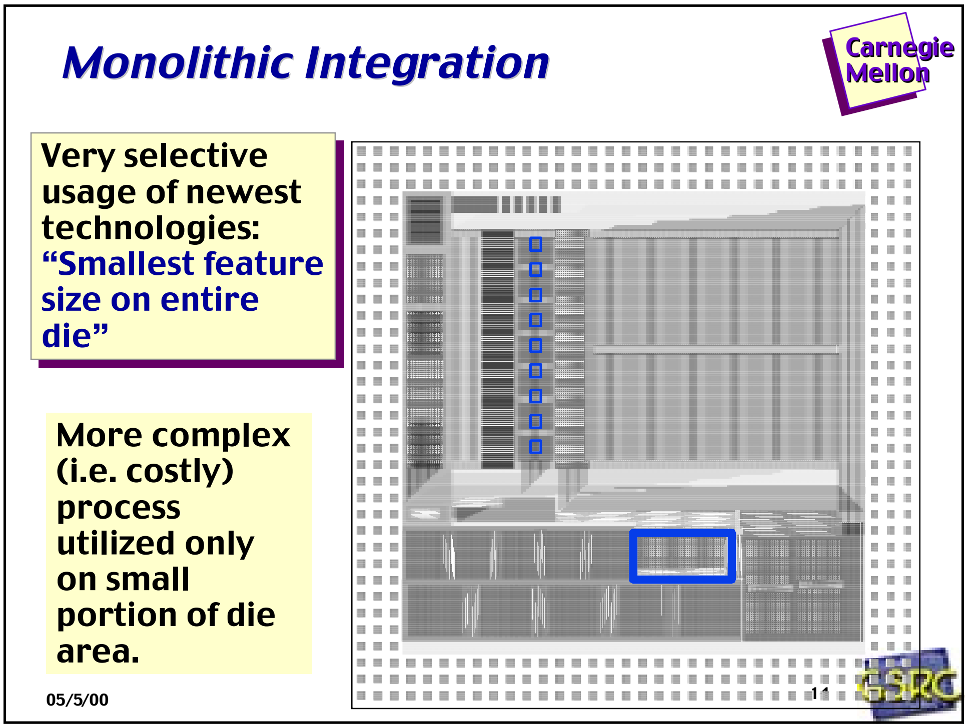


Monolithic Integration

Use of newest technologies: “Cooper and low k” on entire die.

More complex (i.e. costly) process utilized only on small portion of die area.

05/5/00



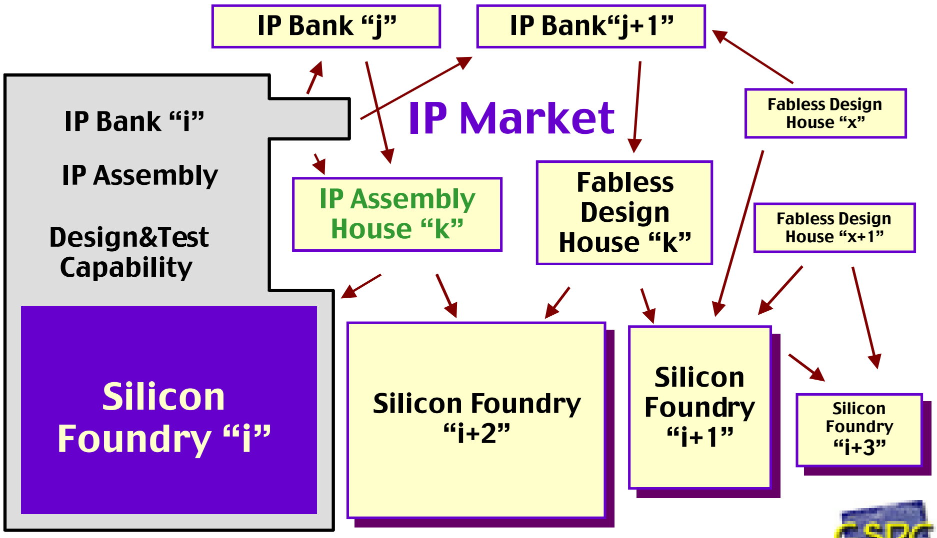
Monolithic Integration

Very selective usage of newest technologies: “Smallest feature size on entire die”

More complex (i.e. costly) process utilized only on small portion of die area.

05/5/00

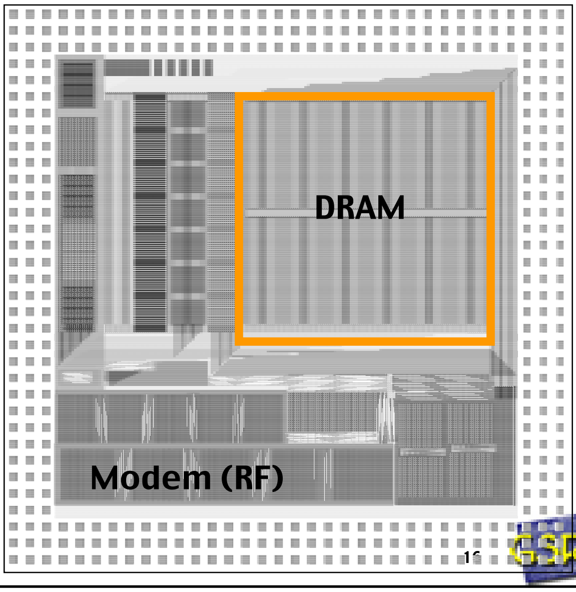
IC Design-Manufacturing Interface : Next 2 –8 Years



Monolithic Integration

Use of IPs from various IP providers and **single silicon provider**

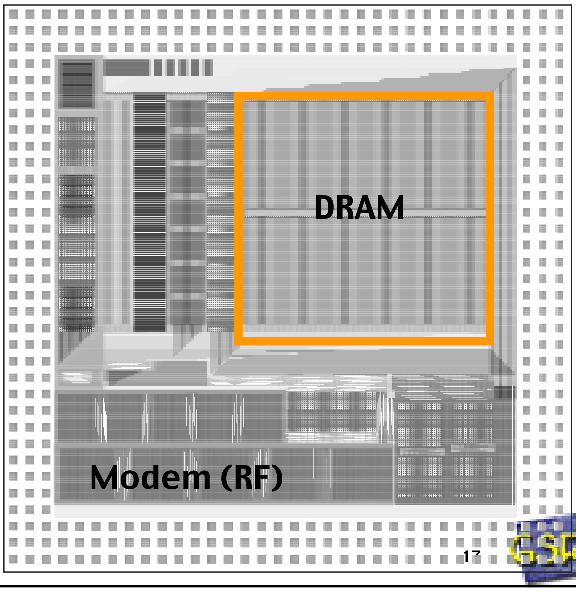
Precludes usage of hard cores from different IP core providers



Monolithic Integration

Very different Electrical environment requirements

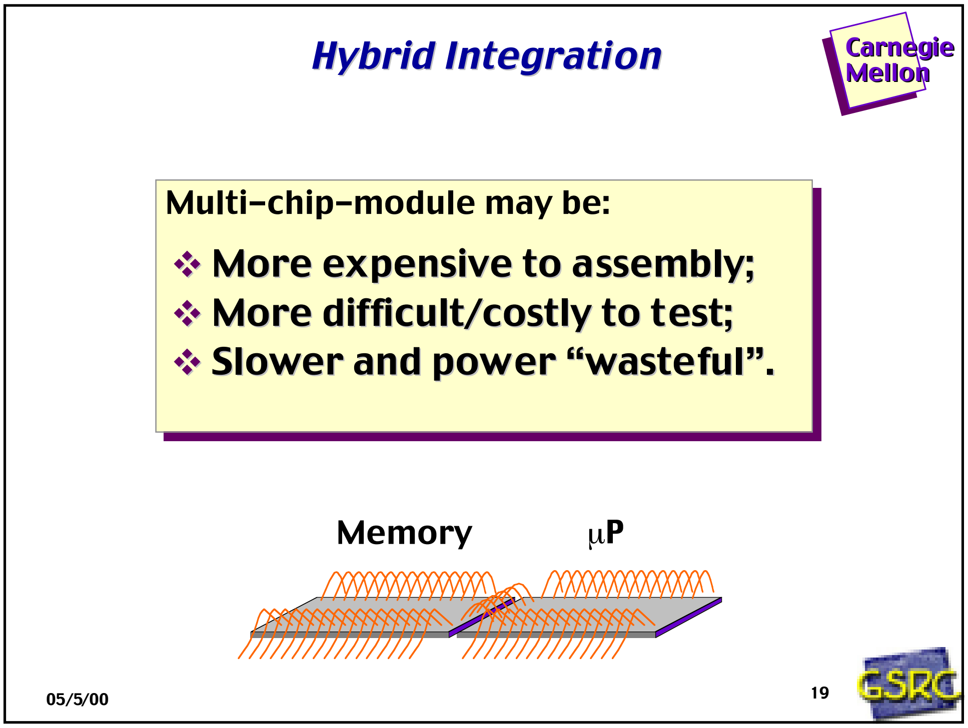
Complex interaction



Monolithic Integration

System-on-chip might be:

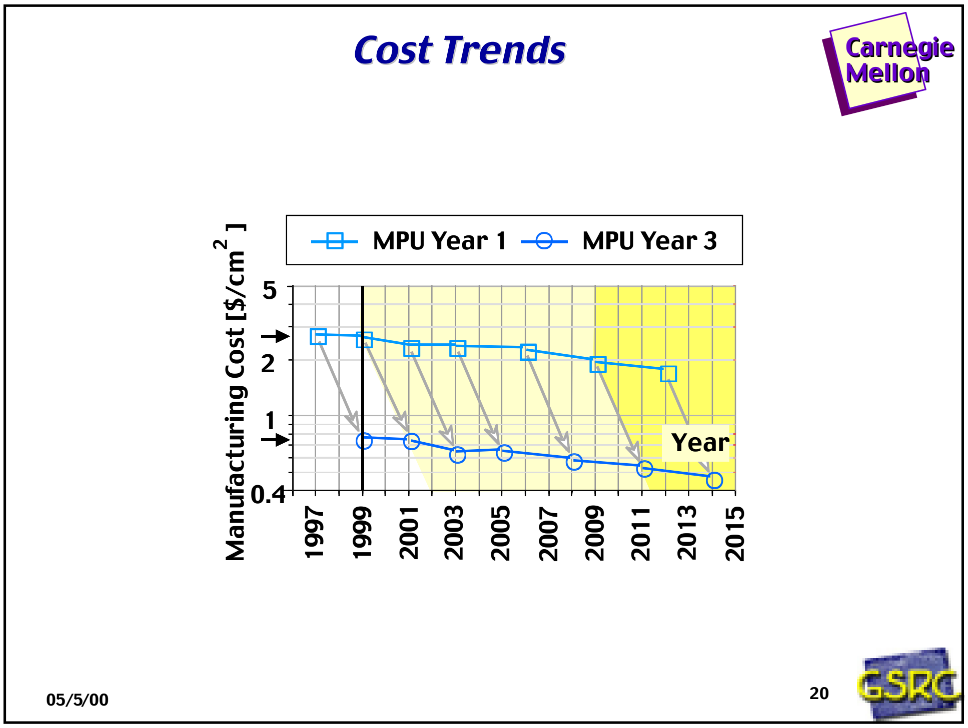
- More expensive to fabricate ! ?
- Incompatible with evolving “IP Assembly Market”
- More difficult to design !
- ....
- ....



Hybrid Integration

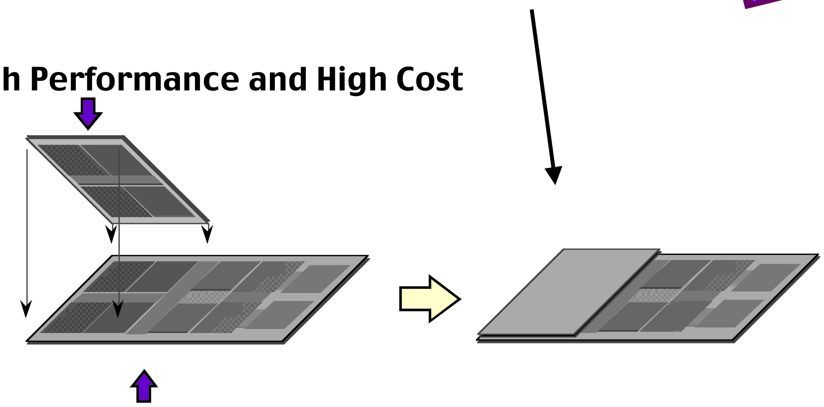
Multi-chip-module may be:

- More expensive to assembly;
- More difficult/costly to test;
- Slower and power “wasteful”.



Cost Trends

2.5 D System Integration



High Performance and High Cost

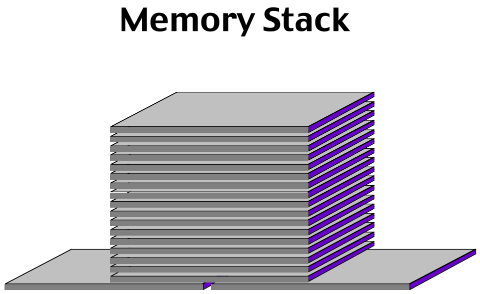
Modest Performance
and Low Cost

2.5 D System Integration : Potential

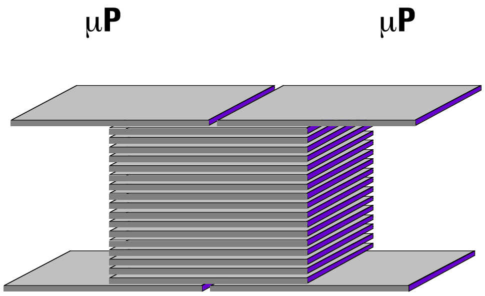
Bus/Memory

μP μP

2.5 D System Integration : Potential



2.5 D System Integration : Potential



2.5 D System Integration :
Potential

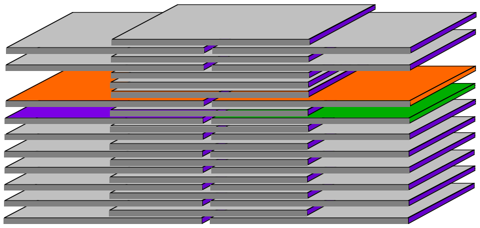
Customer "personalization" layer

My own IP on EEPROM

Analog noise sensitive IP from vendor X

High volume pre-fabricated subsystem

Fastest possible logic from vendor Z

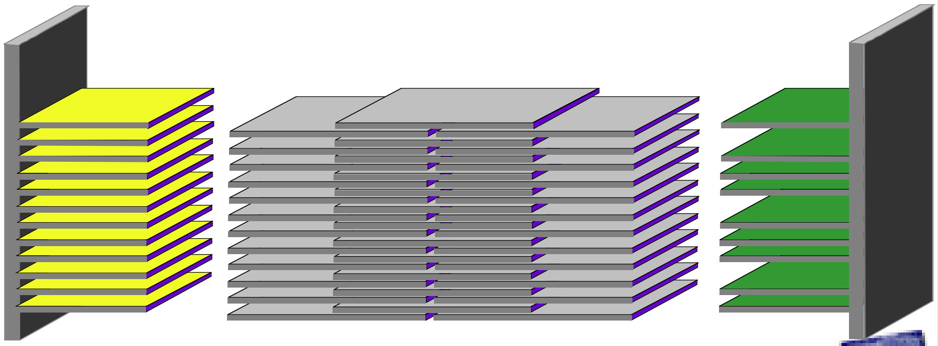


05/5/00

2.5 D System Integration :
Potential

I/Os

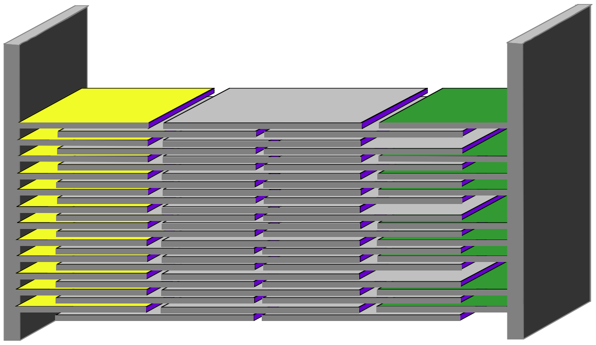
MEMS-based hydraulic cooling system



05/5/00

2.5 D System Integration : Potential

Inexpensive, IP protective, volume fabricated, easily customizable, fast, market ready, expandable, field programmable, ...



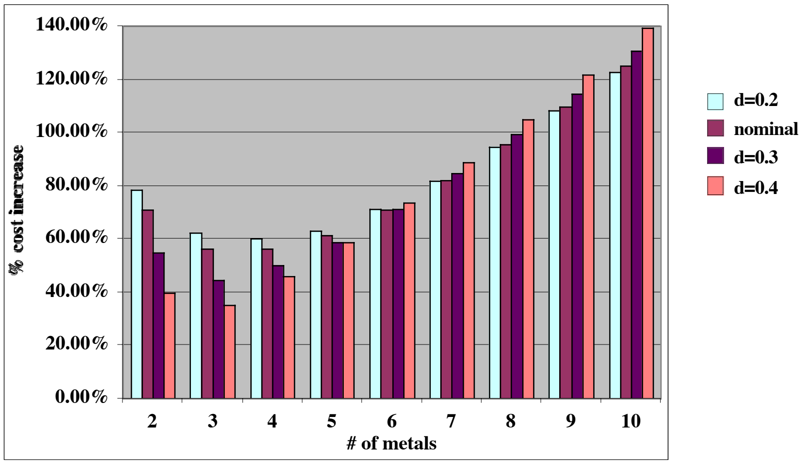
Evolution Trends

How to choose between:
Monolithic and 2.5 D ?
Cost estimation
Performance Estimation

Cost Modeling

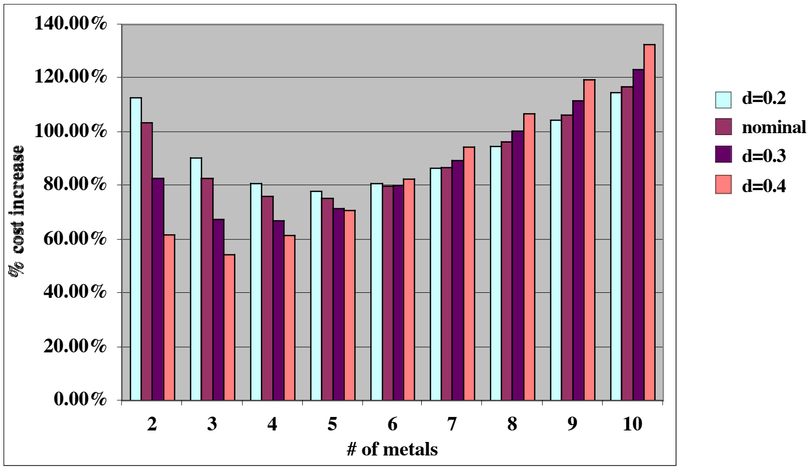
P.K. Nag

Cost Modeling



0.25 micron processes

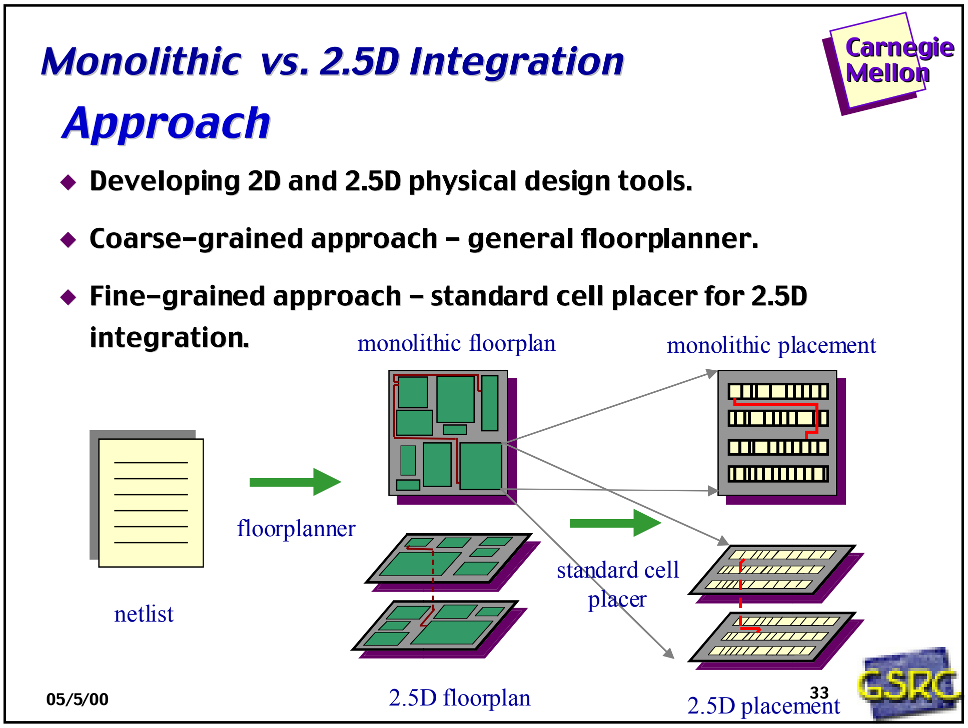
Cost Modeling



0.18 micron processes

2.5 D System Integration : Feasibility Study

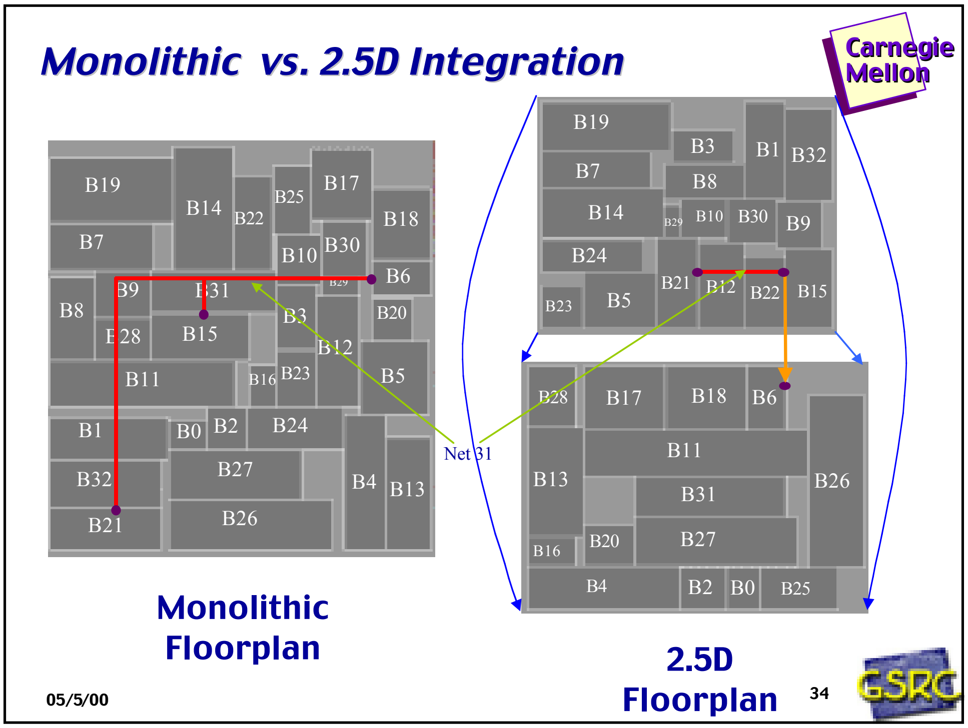
D. Yangdong and P.K. Nag



Monolithic vs. 2.5D Integration

Approach

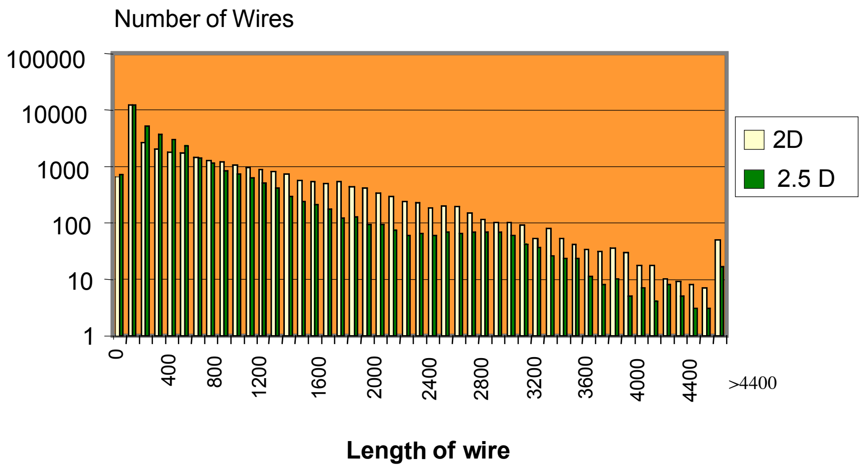
- Developing 2D and 2.5D physical design tools.
- Coarse-grained approach - general floorplanner.
- Fine-grained approach - standard cell placer for 2.5D integration.



Monolithic vs. 2.5D Integration

Monolithic Floorplan

2.5D Floorplan



Monolithic vs. 2.5D Integration

Preliminary Results

- 2.5D integration scheme may offer substantial advantage over traditional monolithic approach.
- For the 2.5D integration scheme to be practical, 2.5D via should be placed on the top of cell area or be very small in size.
- Need for develop fine tuned CAD and manufacturability assessment tools for the 2.5D approach.

2.5 D CAD

Needed tools:

- **Cost modeling for assessment of system integration schema.**
- Placement and routing of two-layer 2.5-D systems
- Placement and routing of entire 2.5-D systems in 3 dimensions.
- Cost-based methodology for system partitioning for 2.5-D systems integration.
- Routing of power distribution of 2.5-D system.
- Modeling of temperature distribution in 2.5-D system.
- Physical design of heat removal systems in 2.5-D systems.

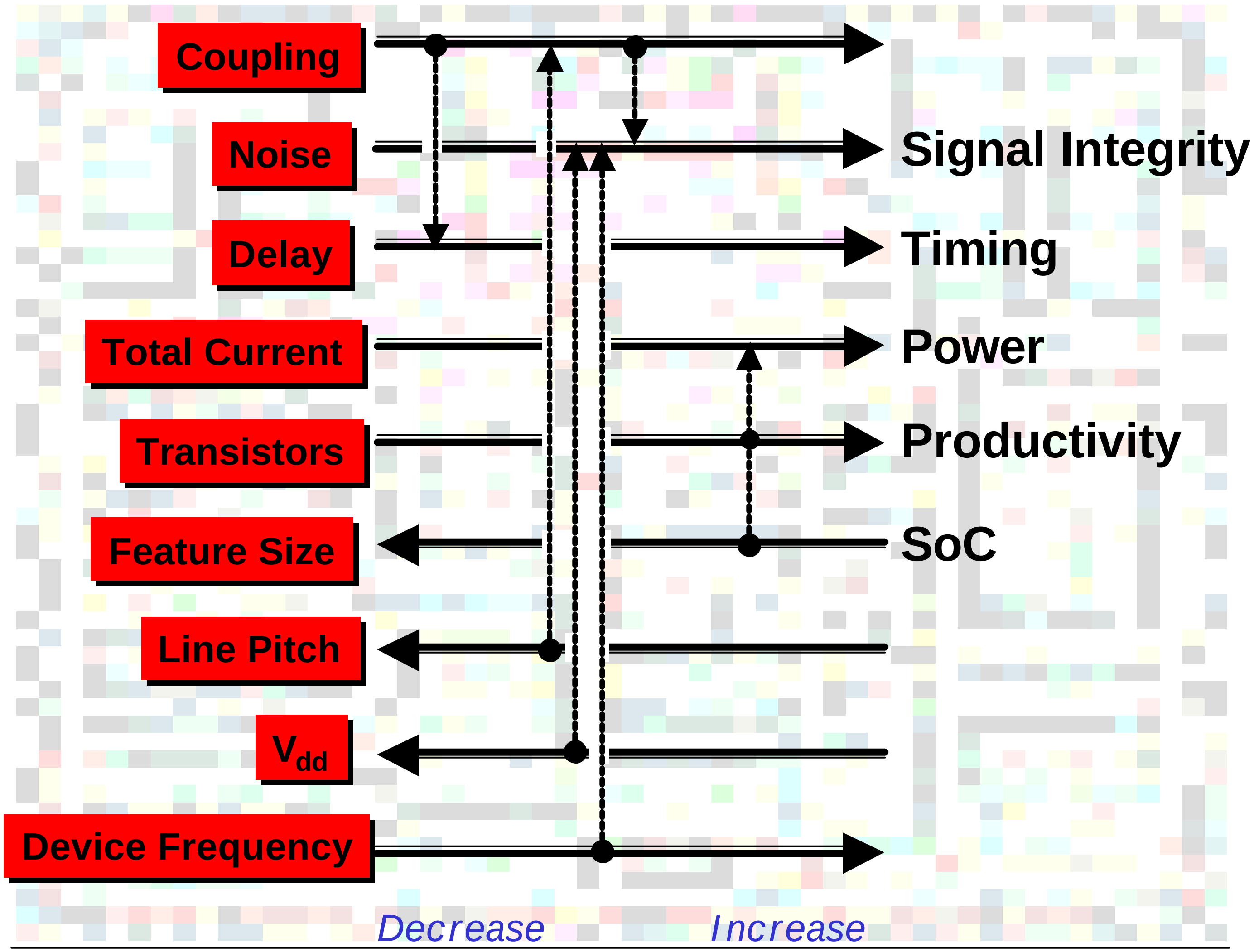
High End IC Design

EDA Roadmap Taskforce Report Design of Microprocessors, 3/99

Donald Cottrell

Si2, Inc.

Areas of Concern



Coupling

Noise

Delay

Total Current

Transistors

Feature Size

Line Pitch

V_{dd}

Device Frequency

Signal Integrity

Timing

Power

Productivity

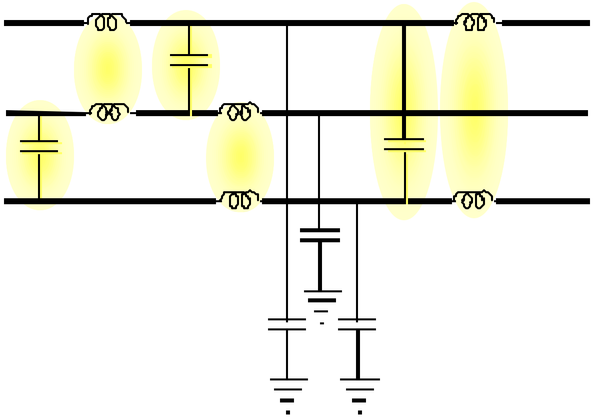
SoC

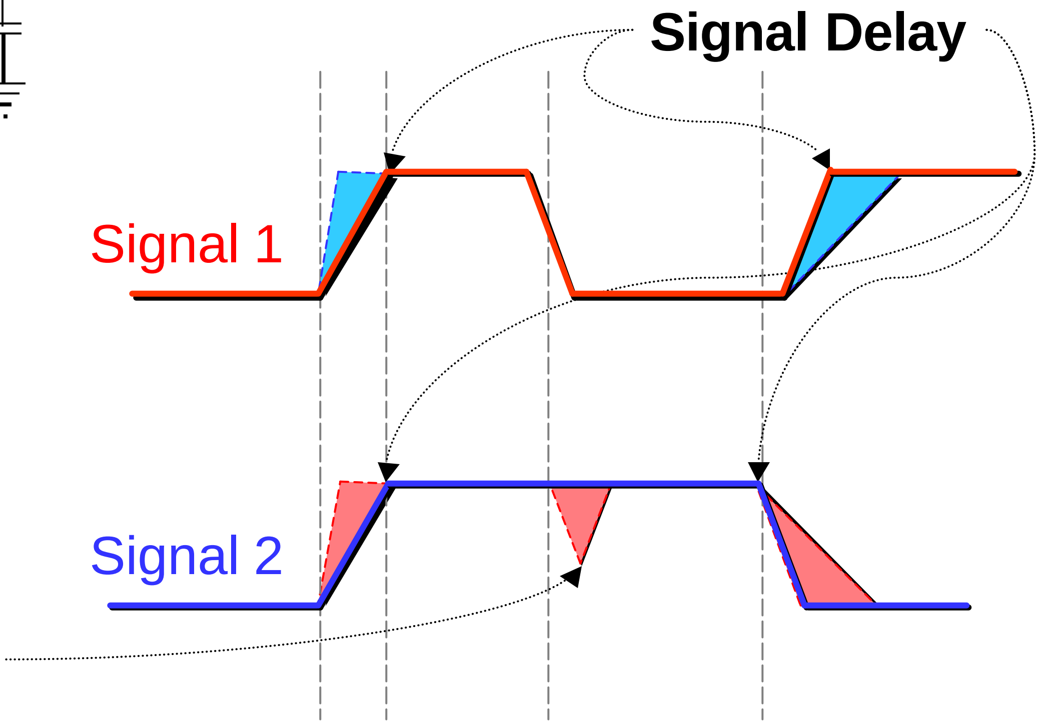
Decrease

Increase

Silicon Integration
Initiative

Coupling (Crosstalk)

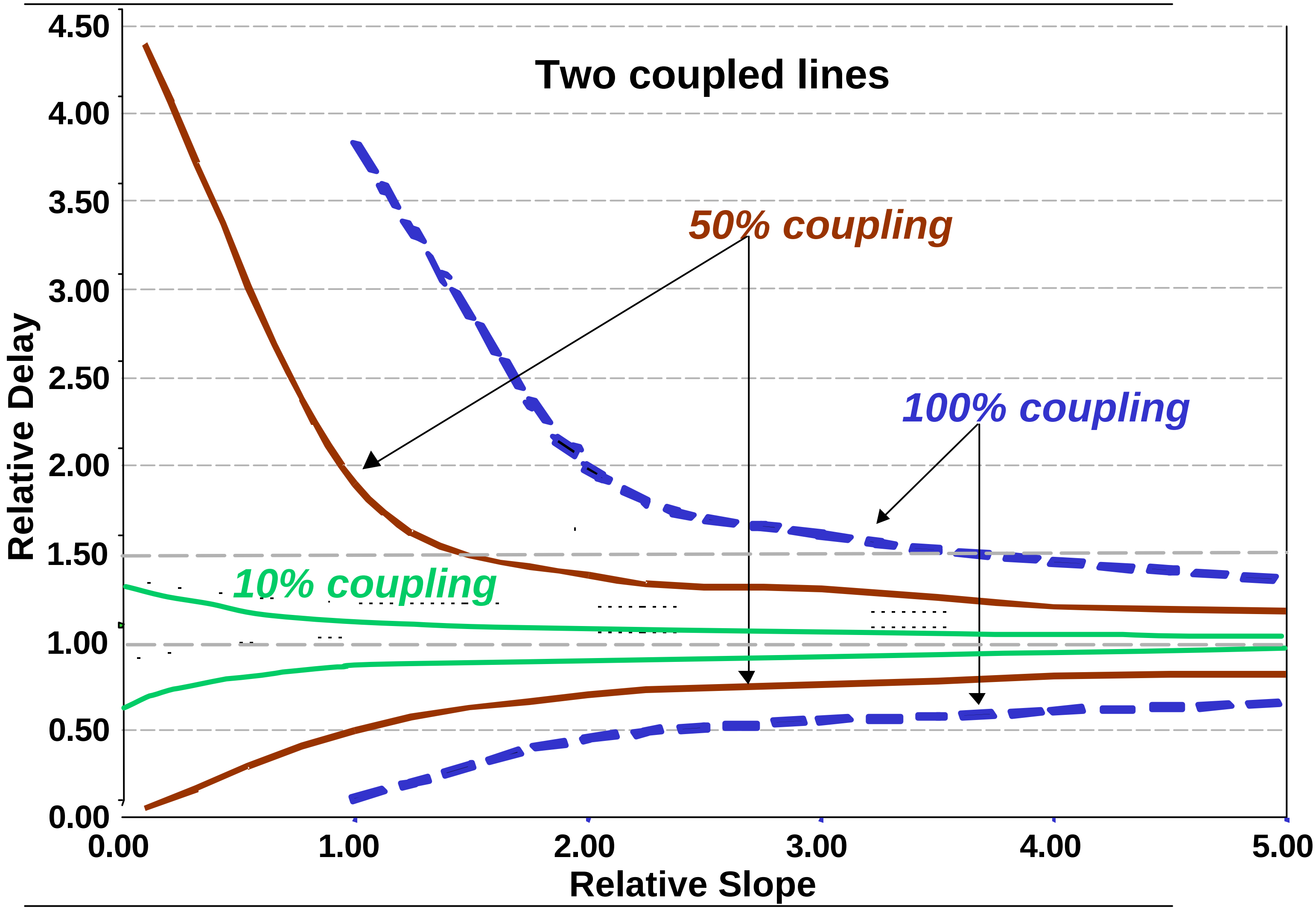




Signal Delay

Noise Spikes

Crosstalk Delay Variation



Source:EDA Roadmap Taskforce Report “Design of Microprocessors”, 1999

Signal Integrity Concern Areas

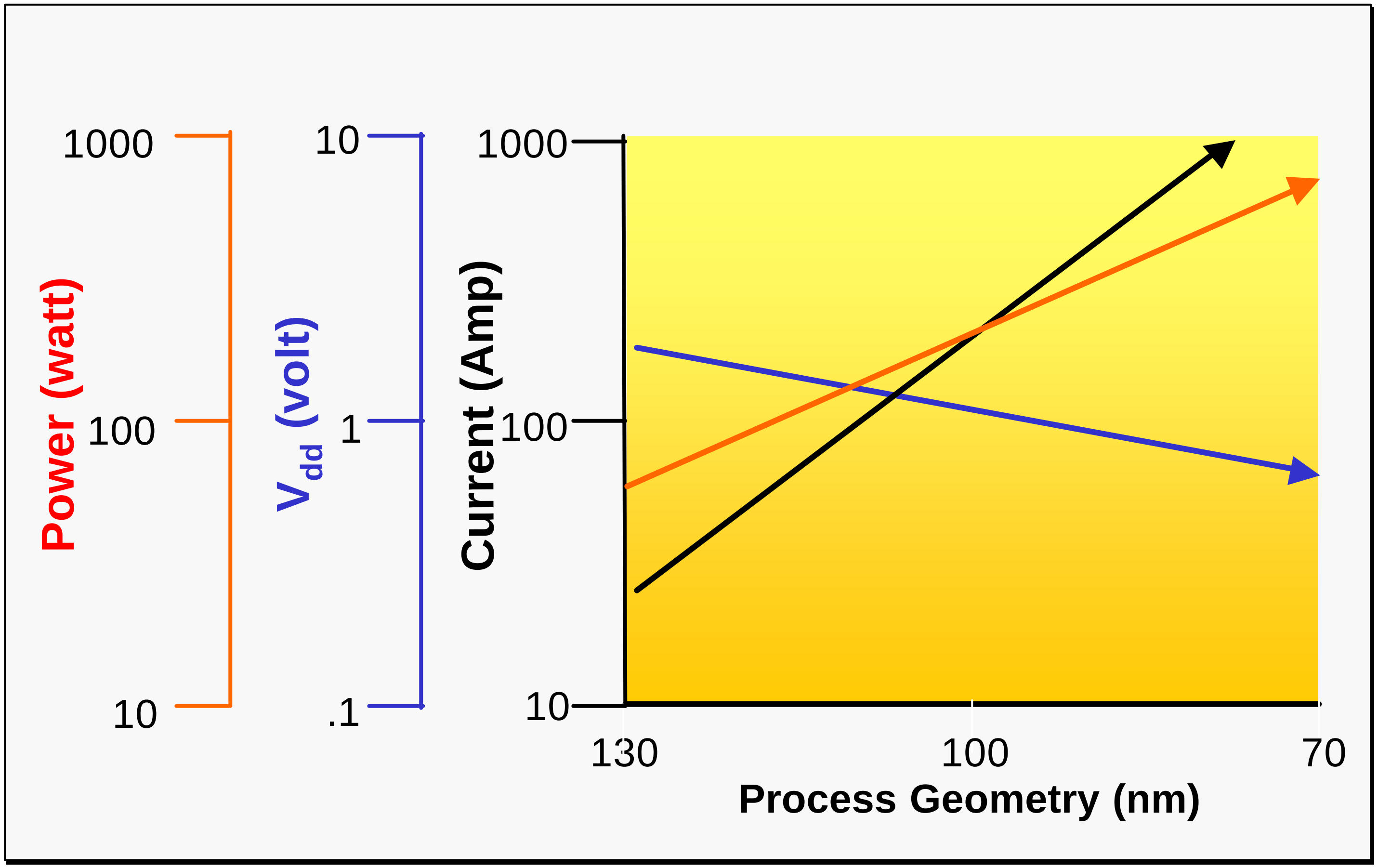
- **Pattern dependant analysis vs. guard banding**
- **Effects of ECs on unchanged portions of design**
- **Determination of Effected Nets**
  - Global nets
  - BUSS structures
  - Power grid with very large *di*/*d*t
- **Substrate coupling**
- **Soft Errors**

Signal Integrity Recommendations

- **Semiconductor Process Changes**
  - Additional Metal Layers for Shielding
  - Low mutual capacitance and low mutual inductance between signals, including power
- **Design Methodology**
  - Hierarchical Design that is Interconnect-centric
  - Staggered Signals
- **Design Automation**
  - Noise Aware Design Tools (e.g.Physical Design)
  - Multi-Port Delay Models
  - Multi-Path Timing Analyzer
  - Tools for asynchronous design
  - Critical Net Identification (Noise, Lumped vs. Distributed)

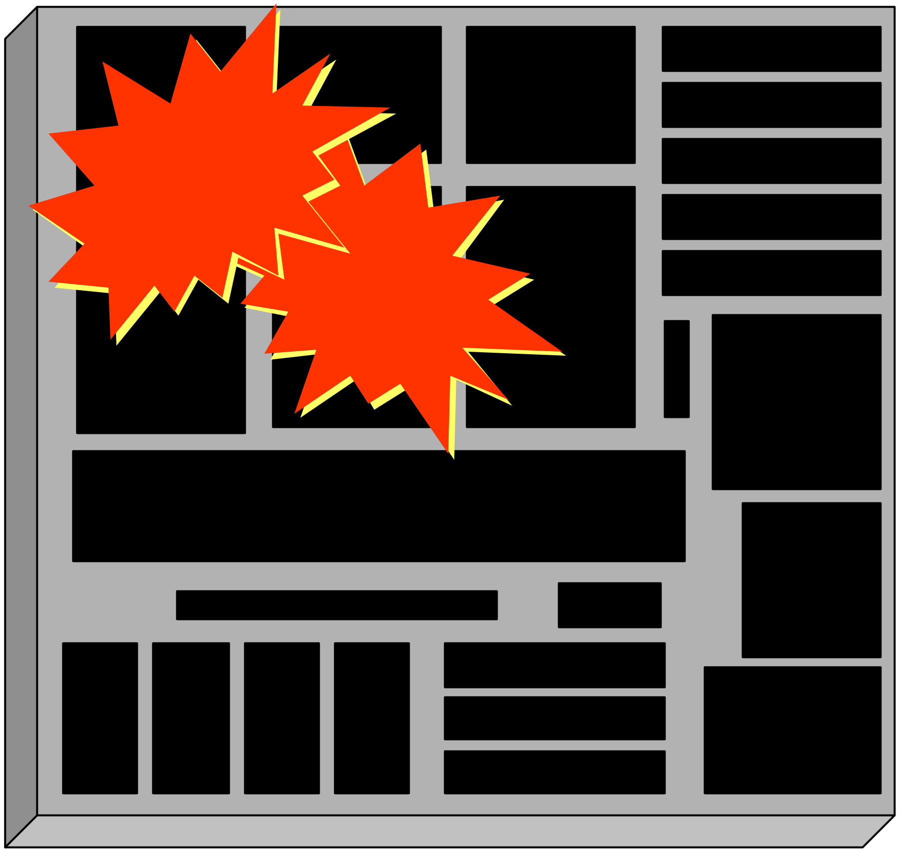
Silicon Integration Initiative

Power



Source:EDA Roadmap Taskforce Report “Design of Microprocessors”, 1999

Power Concern Areas



Hot Spots
  Delay = f (Temp)

Ldi/dt noise

IR Drop

Current Density
  Electromigration

HW/SW Tradeoffs

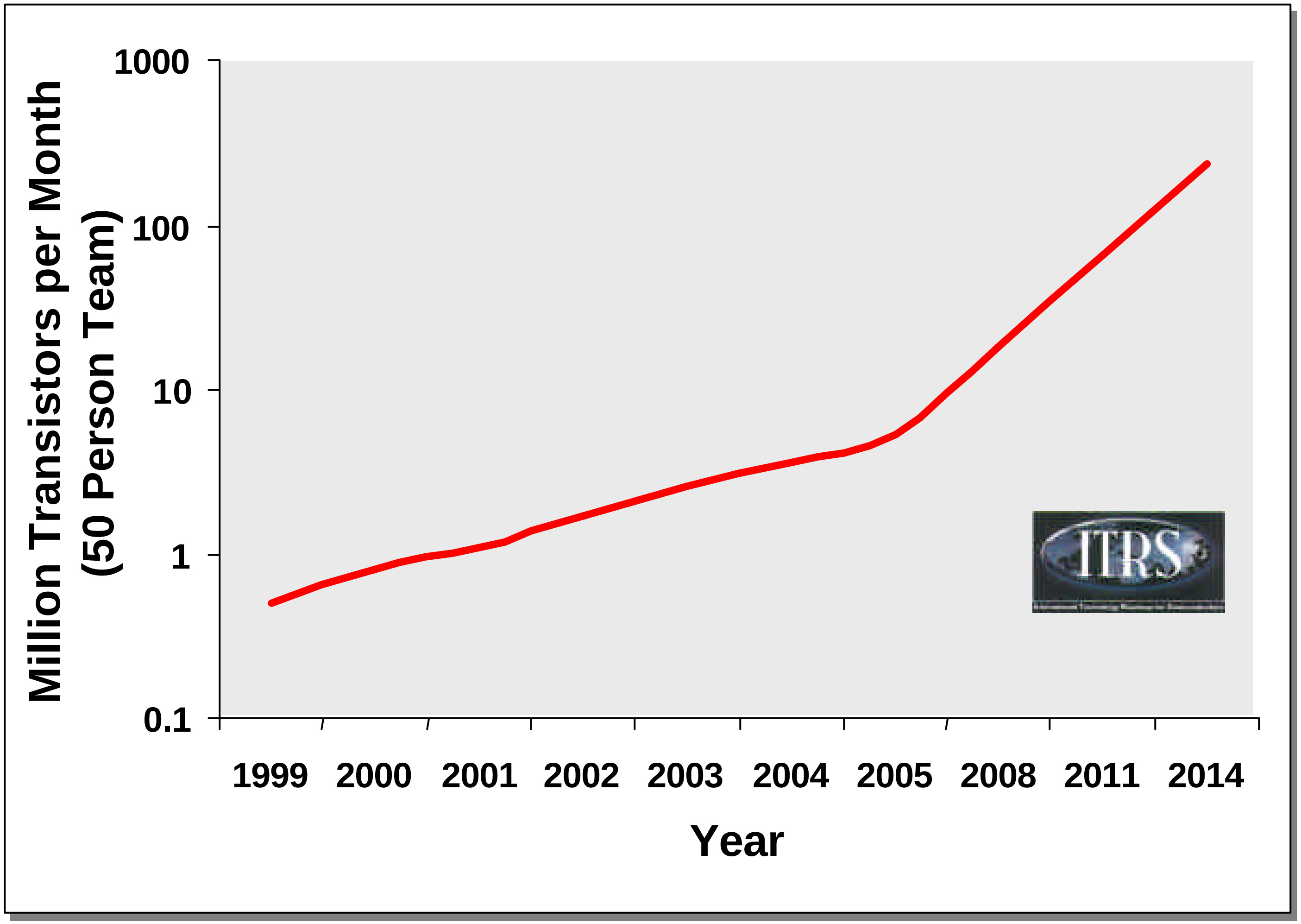
Silicon Integration Initiative

Power Recommendations

- **Semiconductor Process Changes**
  - Additional Metal Layers for Power Planes
  - Additional Metal Layers for Shielding
  - On Chip Decoupling Capacitors
- **Design Methodology**
  - Increase Usage of Gated Clocks
  - Staggered Clock
  - Self Timed and Asynchronous Design
- **Design Automation**
  - Early Prediction of Power (Architectural/RTL/Gate)
  - Hardware-Software Power Analysis Tools
  - Power Dependent Timing Verification
  - Noise Analysis Tools (Inductive Coupling, IR Drop)

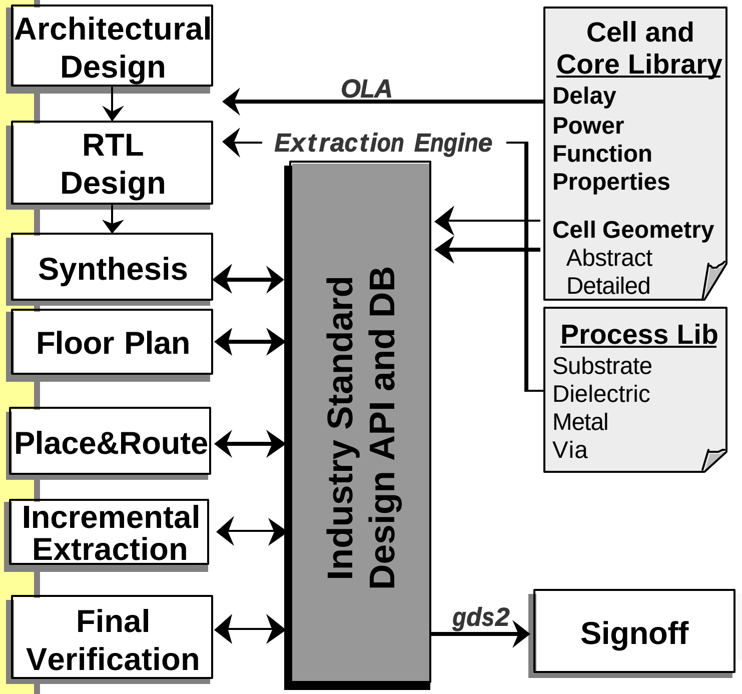
Silicon Integration Initiative

Design Productivity



EDA System Recommendations

- Higher level design tools
  - Function, Performance, Power, ..
  - Followed in lower levels by:
    - Assertion driven design
    - Equivalence checking
- Constraint driven design tools (power, timing, signal integrity, …)
- Incremental Analysis and Optimization
- Concurrent design and analysis
- Integration via Open Architecture
  - Industry Standard data model
  - Industry Standard data interface
- Forecast/Audit
- Model Builders



Architectural Design

RTL Design

Synthesis

Floor Plan

Place&Route

Incremental Extraction

Final Verification

Industry Standard Design API and DB

OLA

Extraction Engine

gds2

Signoff

Cell and **Core Library**
Delay
Power
Function
Properties
Cell Geometry
Abstract
Detailed

Process Lib
Substrate
Dielectric
Metal
Via

Giga = 1/nano

CAD Challenges for Giga-scale Mixed Technology Micro Systems

Steven P. Levitan & Donald M. Chiarulli
University of Pittsburgh

steve@ee.pitt.edu & don@cs.pitt.edu

Acknowledgements

- Timothy P. Kurzweg
- Jose A. Martinez
- Eric N. Reiss
- Philippe J. Marchand (OMM)
- http://kona.ee.pitt.edu/pittcad

DARPA

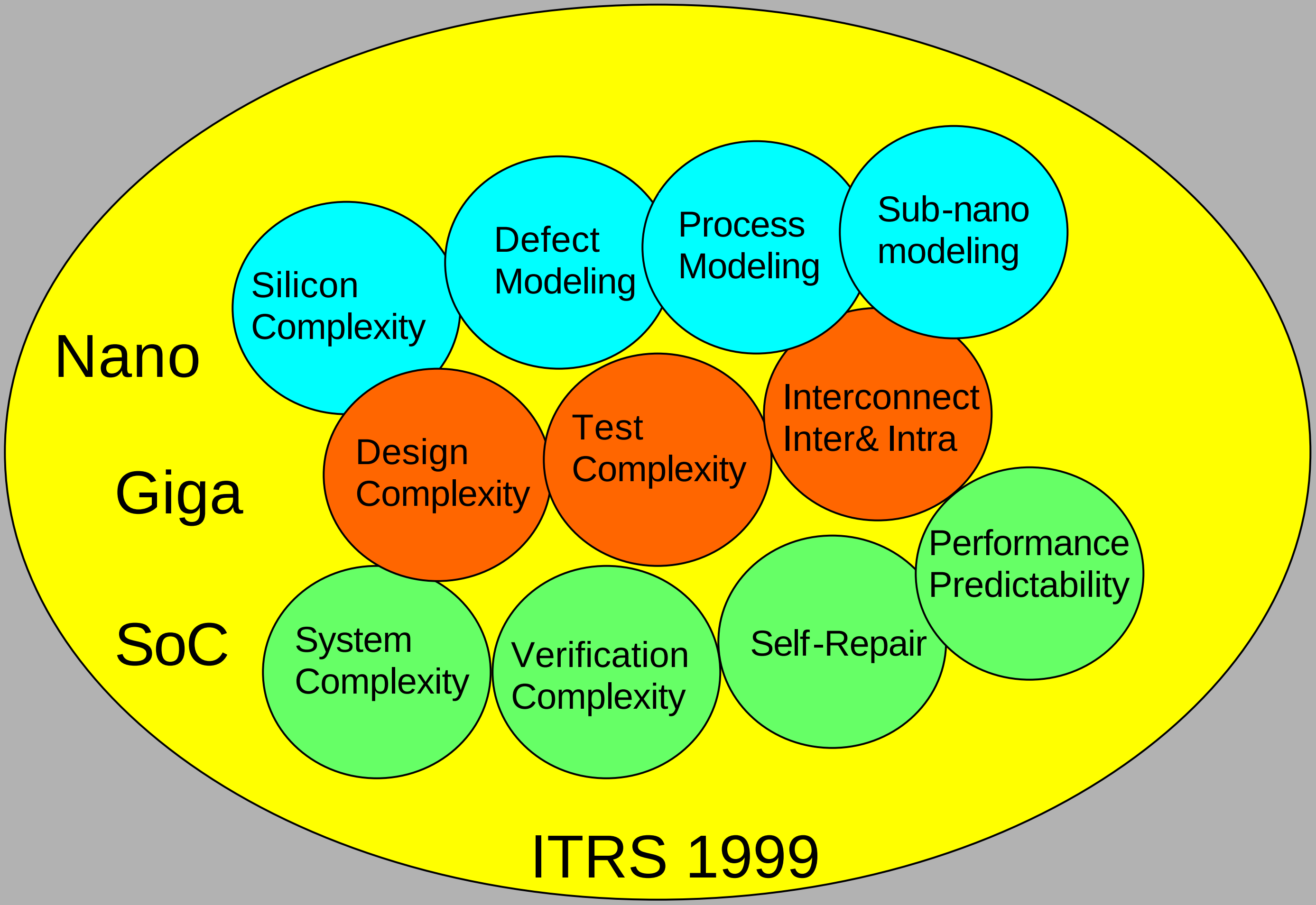
3-D OE SP

UNIVERSITY OF CALIFORNIA · SAN DIEGO ·

NSF

CHATOYANT

Where the Problems Are



Nano

Giga

SoC

Silicon Complexity

Defect Modeling

Process Modeling

Sub-nano modeling

Design Complexity

Test Complexity

Interconnect Inter& Intra

Performance Predictability

System Complexity

Verification Complexity

Self-Repair

ITRS 1999

Size Based Problems - nano

- The obvious:
  - Small scale device modeling
  - Interconnect modeling
  - Limits to shrinking features, voltages, etc.
- Why:
  - We have been riding a curve - and reaping the benefits of technology improvements not of our own making
  - There has been an acceleration of technology introduction

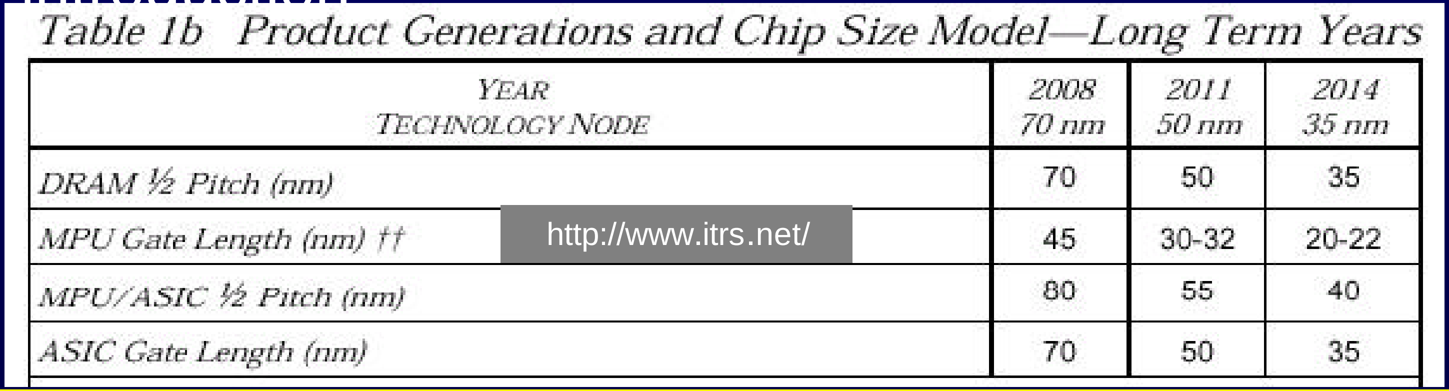


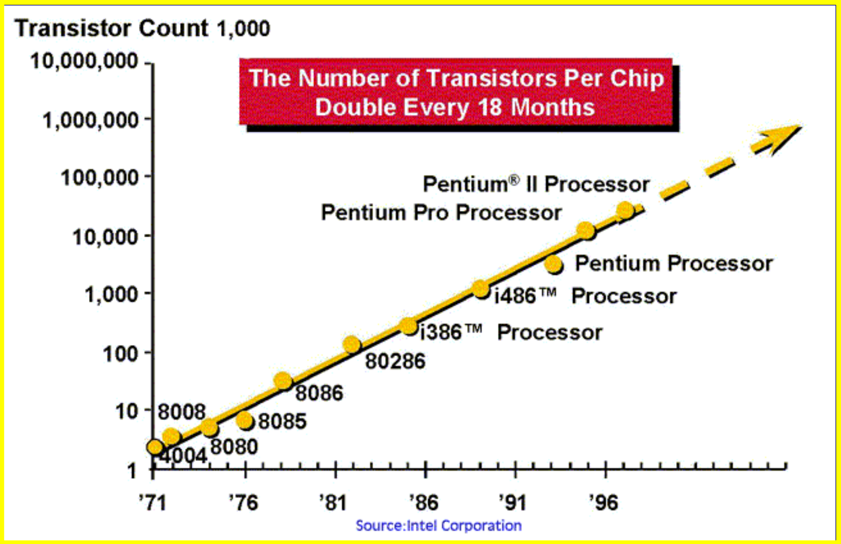
Table 1b Product Generations and Chip Size Model—Long Term Years

YEAR TECHNOLOGY NODE	2008 70 nm	2011 50 nm	2014 35 nm
DRAM ½ Pitch (nm)	70	50	35
MPU Gate Length (nm) ††	45	30-32	20-22
MPU/ASIC ½ Pitch (nm)	80	55	40
ASIC Gate Length (nm)	70	50	35

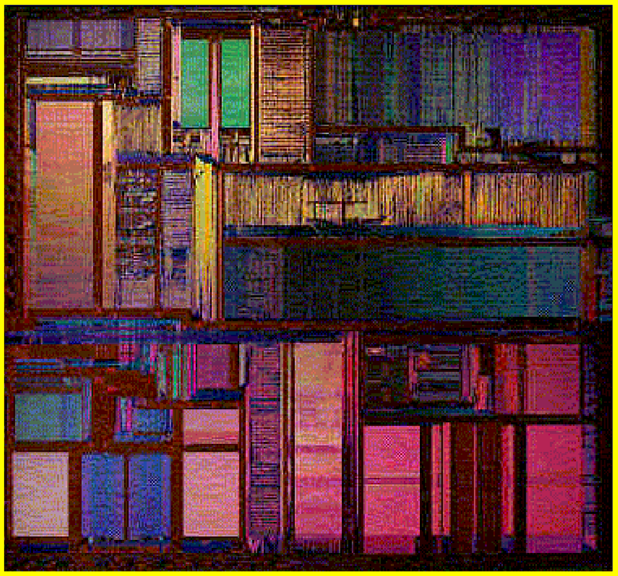
http://www.itrs.net/

Scale Based Problems - giga

- The obvious:
  - Design complexity
  - Design interactions
  - Modeling problems - both accuracy and speed
- Why:
  - More devices with shorter time to market
  - IP based solutions - problems
  - Large physically distributed design teams



Source:Intel Corporation



http://www.intel.com

SOC's (Multi-Domain)

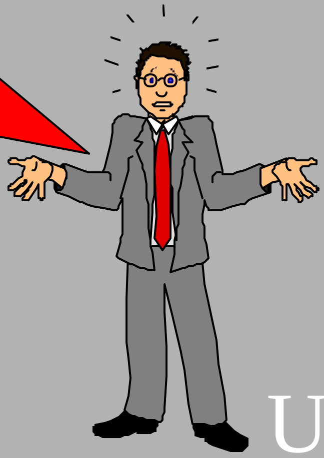
- The obvious:
  - – IP Libraries
  - – Analog, mixed signal
- However:
  - – Multi-domain, Multi-IP projects are hard to do well
  - – Why does anyone think that libraries will work this time?
    - – Not for SW or HW
    - – Therefore ... should work for SOC?
  - – Smaller/Faster/Cheaper "did not work" - why?

http://www.nasa.gov

Where the Problems *Really* Are

Nano/Giga/Soc
ITRS 1999

- As any designer knows, it's the un-anticipated problems which are the real "gotcha's"
- So, what is ***NOT*** in the ITRS roadmap

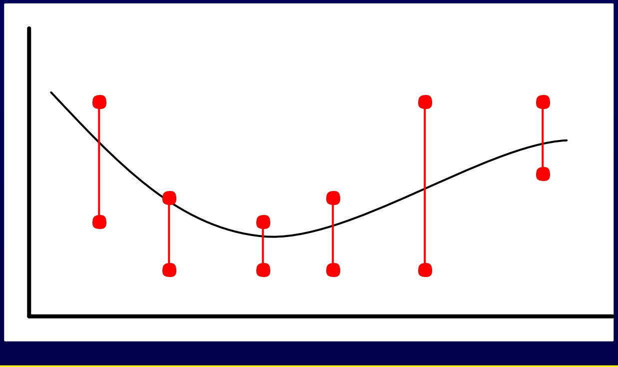


What’s Missing?

- Need to know “how good” we have to be
  - Trade off accuracy vs. speed of simulation
  - But: How much accuracy is needed?
- Need to understand mixed technology interactions
  - Not just substrate noise and ground bounce
  - Crosstalk of signals in every domain and even between domains
- Need to integrate reliability models into the design process
  - Its not just *performance* optimization any more...

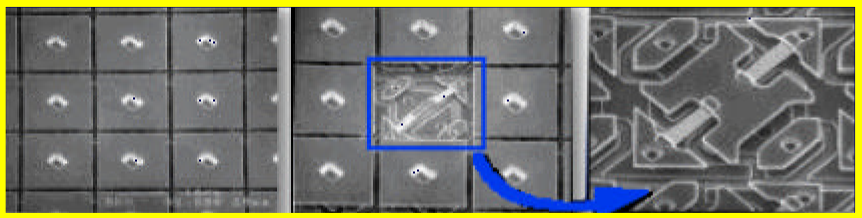
How Good is Good Enough?

- To find the *UNEXPECTED* problem
  - Design analysis must be “detailed enough”
  - *AND* cover all aspects of the system
- Current solution paths lead to complex models of complex systems
  - Accurate models (nano) of big systems (giga)
  - Hard to model, simulate, and evaluate the results
- Error estimation applied in parallel with simulation
  - System simulation results can be presented as a dual product of value plus error bound

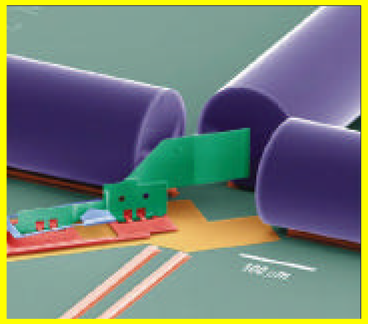


Mixed Domain Effects

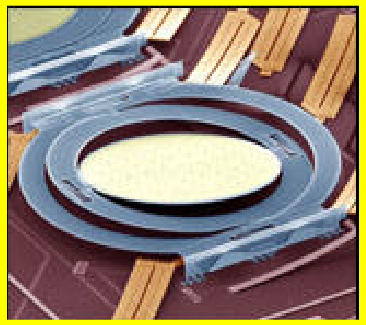
- Real systems have inputs from and outputs to the real world, not USB ports to printers
  - Analog, Optical, Mechanical, Chemical, Biological signals - not just I/O
- "Crosstalk" both within and between domains
  - Interaction of domains with temp, fatigue, operation
  - Tolerancing, mechanical deformations.
- Material incompatibilities



Texas Instruments - http://www.ti.com/dlp



Bell Labs- http://www.bell-labs.com/

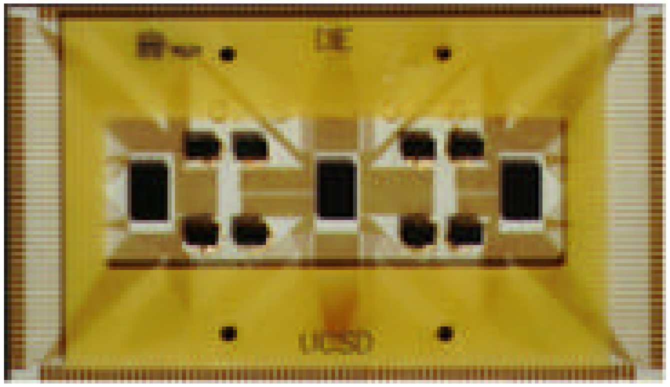


Lucent - http://www.lucent-optical.com/

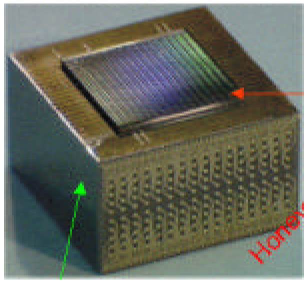
Reliability (and Testing)

- Performance measures:
  - Traditional: speed, power, area, cost ...
  - Need: noise, crosstalk, soft errors (e.g., alpha particles) failure rates...
- Leads to reliability of systems - not just components
- Need imbedded error checking, correcting and repair
  - We need to model it too
- Fault models and testing for mixed technology devices?
  - Clueless

3DOESP

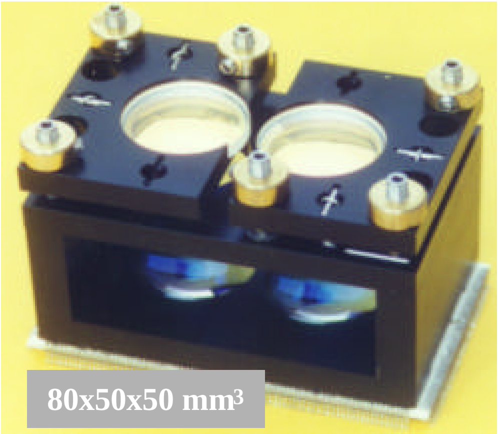


Board Level Packaging

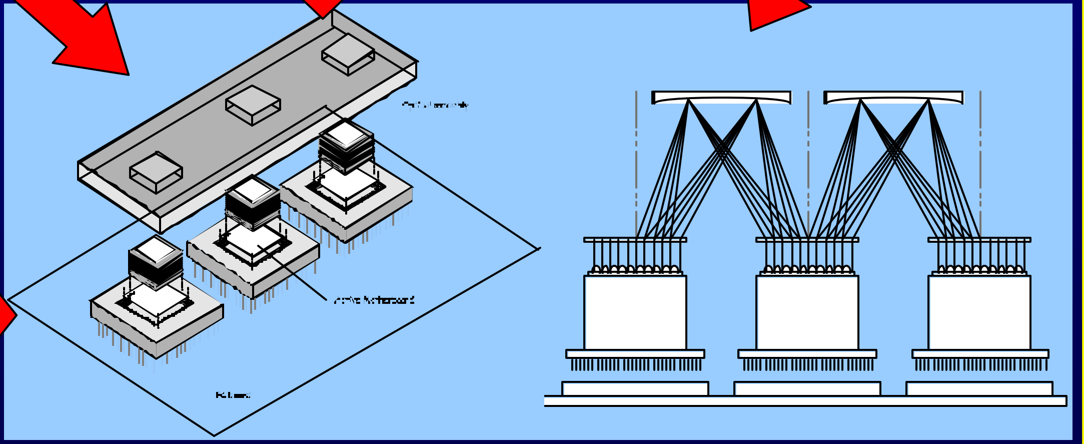


Stacks

Chatoyant



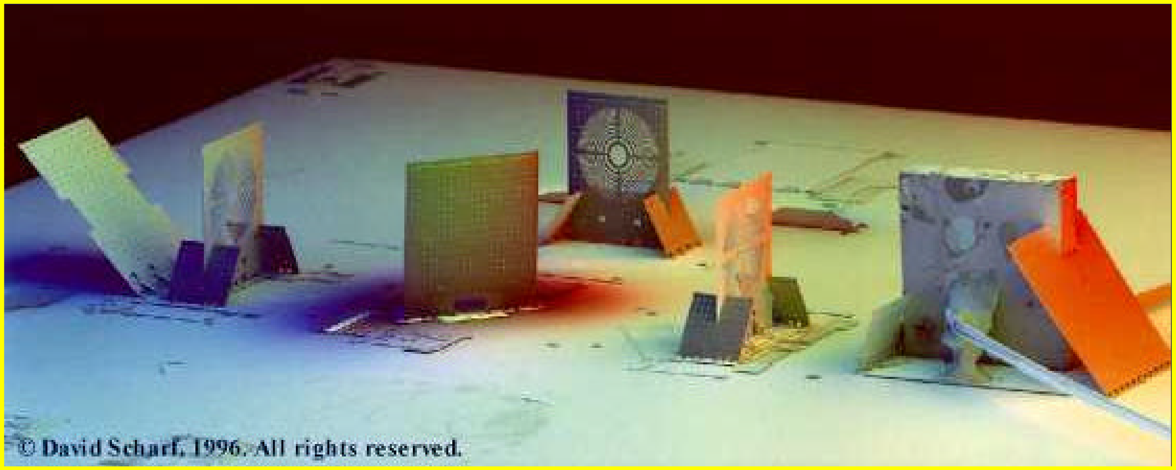
Vertical Optics, Passive Assembly



Final System Demonstrator: 256 Gbit/sec crossbar switching, < 100 W, < 150 cm³

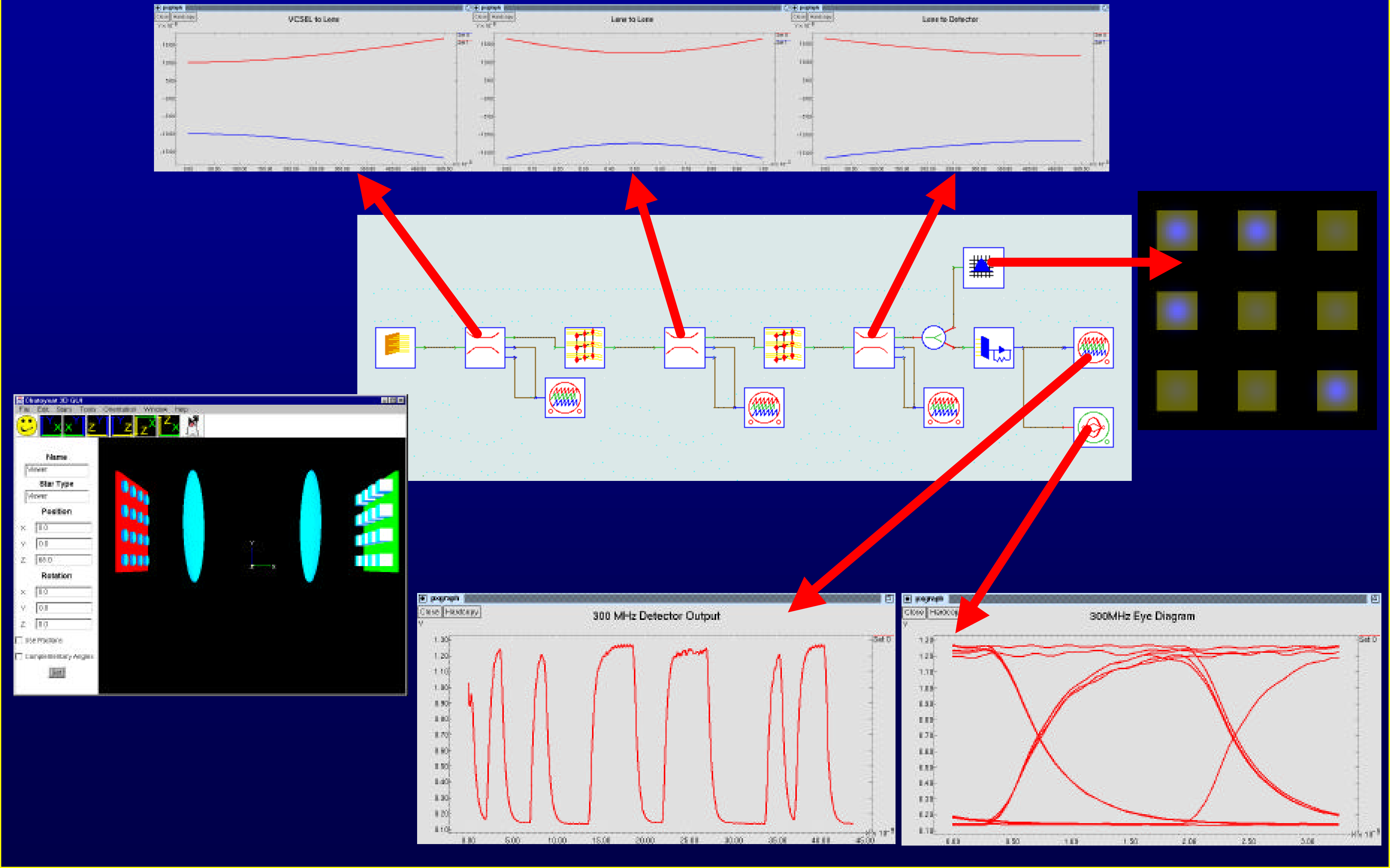
Optoelectronic System Level Design

4 Domains				Interactions	
Electronics	Opto-electronics	Optics	Mechanics	Tolerancing	Performance
Functional - VHDL	Analytic Models	Image Formation	Positions, Angles	Mis-alignment	Digital: Correctness
Logic - SPICE	Physical Models & Experimental Data Fitting	Gaussian Beam Propagation	Movement	Noise & Crosstalk	Analog: BER, Speed
Circuit	Numerical & Statistical	Diffraction Analysis	Inertia & Deformation	Multi-Domain Interactions	Power/Size/ Cost

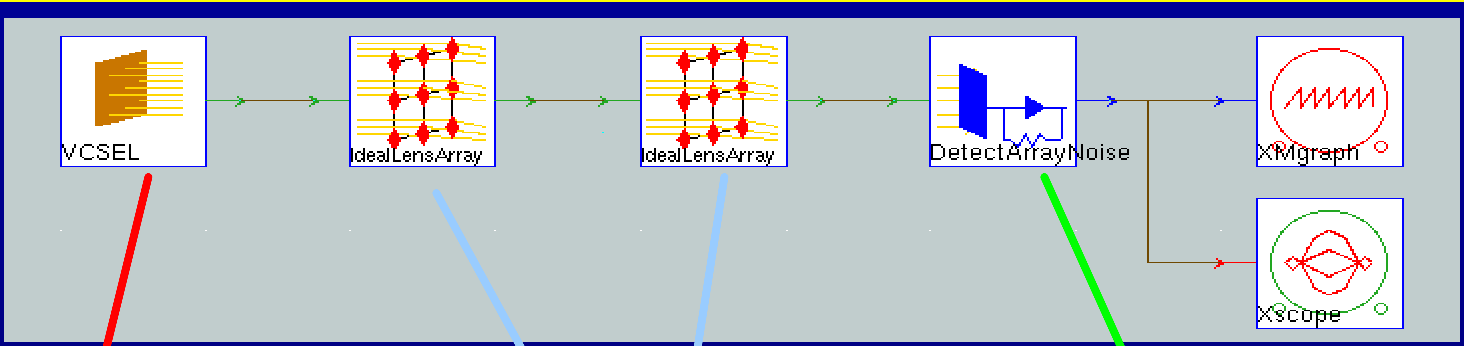

© David Scharf, 1996. All rights reserved.

UCLA - Free Space MicroOptical Bench (FS-MOB) - http://www.ee.ucla.edu/labs/laser/

Chatoyant

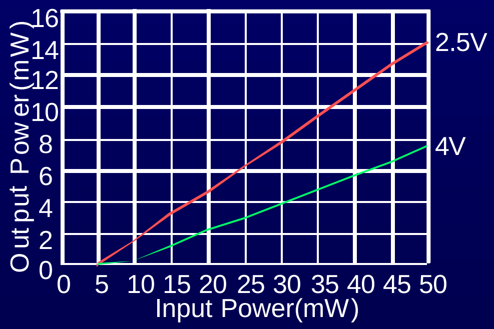

VCSEL to Lens
Lens to Lens
Lens to Detector
Chatoyant 3D GUI
File Edit Stars Tools Orientation Window Help
Name
Star Type
Position
X
Y
Z
Rotation
X
Y
Z
300 MHz Detector Output
300MHz Eye Diagram
Close
Hardcopy

Component Models



Empirical models

Experimental data fitting



$$P_{out} = \frac{h_{LI}/V_{th}}{(1-h_{LI}/V_{th})}(P_{in} - I_{th}V_{th})$$

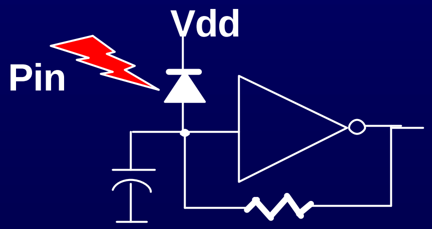
Analytic models

Physics based

$$I(r,z) = I_0\left[\frac{W_0}{W(z)}\right]^2 \exp\left[-\frac{2r^2}{W^2(z)}\right]$$

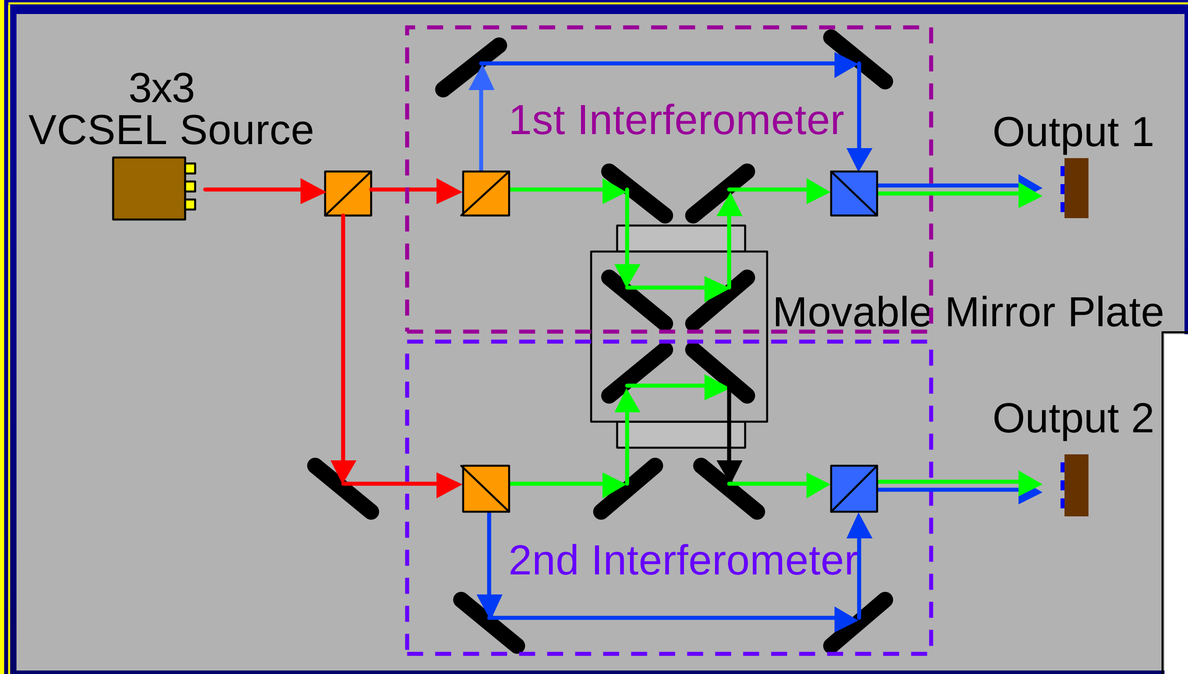
Derived models

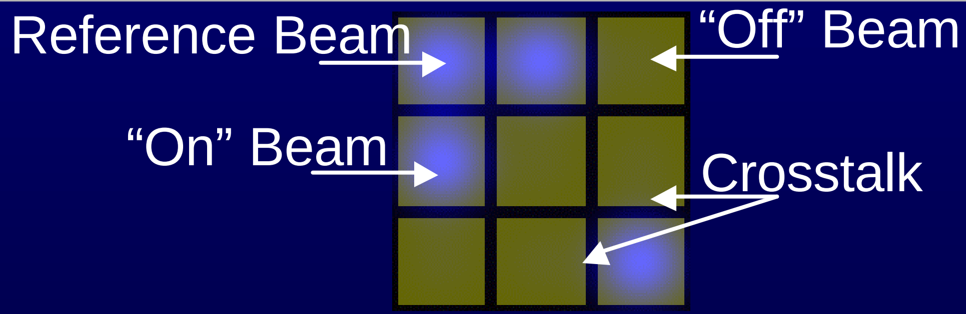
Parametric models extracted from or verified by lower level tools



$$V_0(s) = \frac{R_f}{1+\left(\frac{R_f C}{A}\right)s} \cdot P_{optic}(s)$$

1x2 Optical MEM Switch

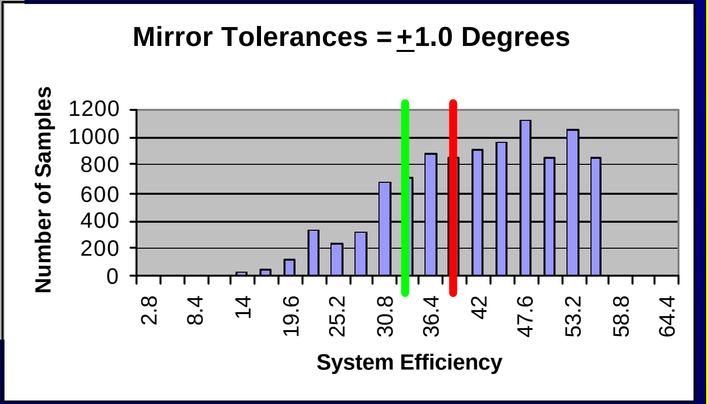


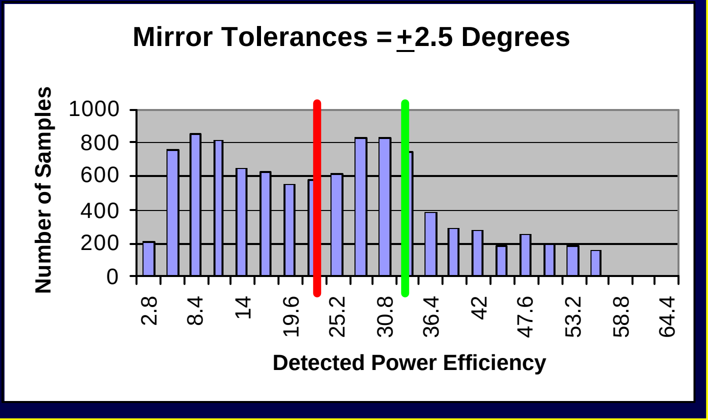


- 56% efficiency
- -15.5 dB worst case neighboring crosstalk

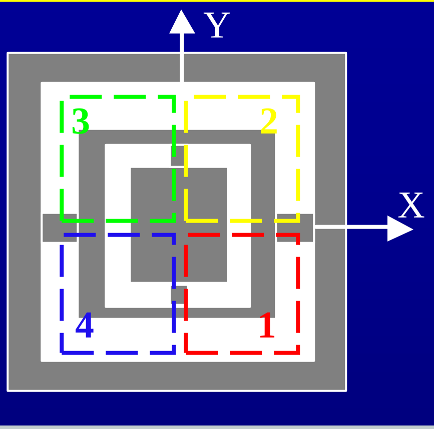
Monte Carlo Analysis

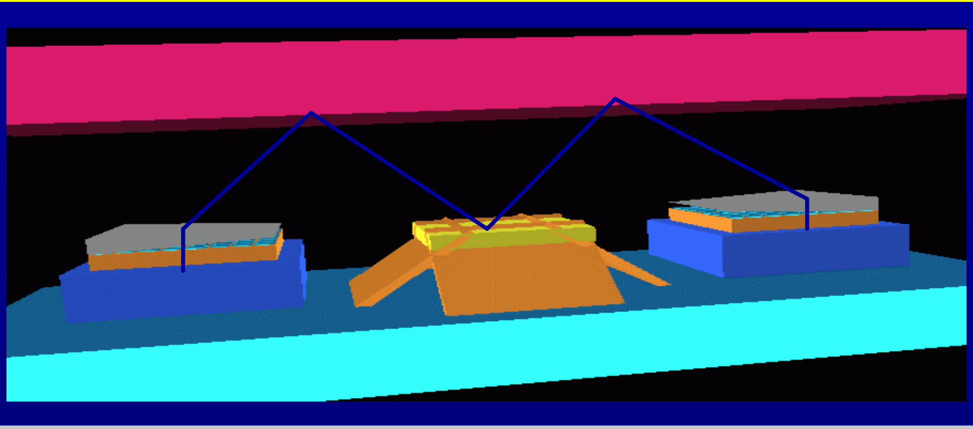
- –Average efficiency
- –33% efficiency

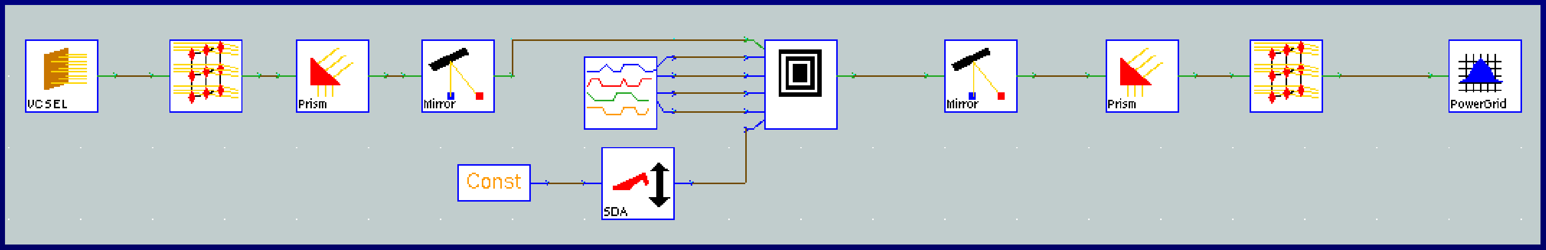


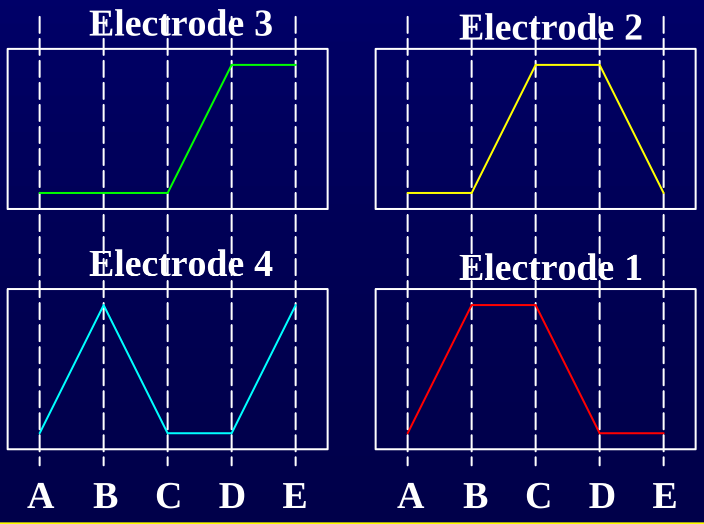


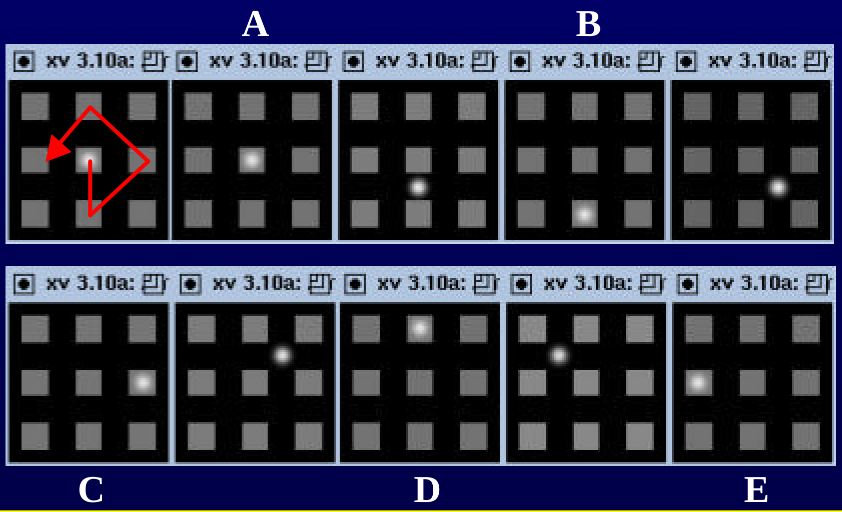
Beam Steering with Torsion Mirror





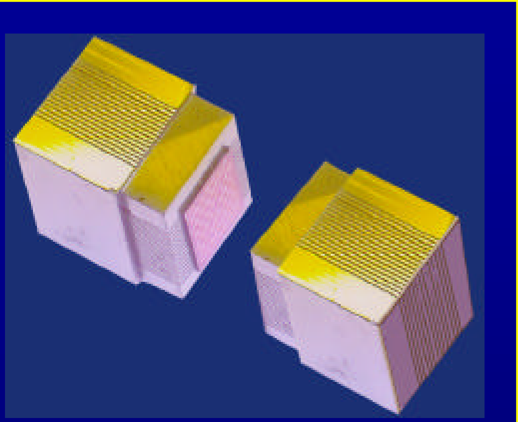




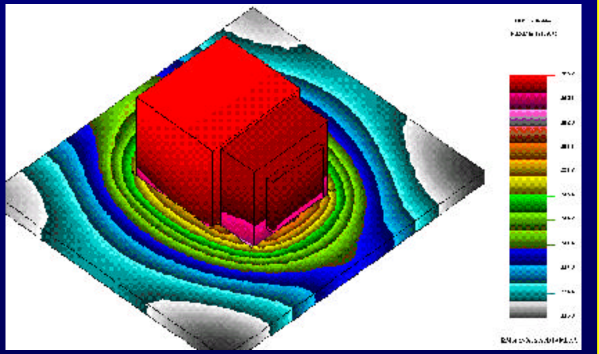


What did we learn?

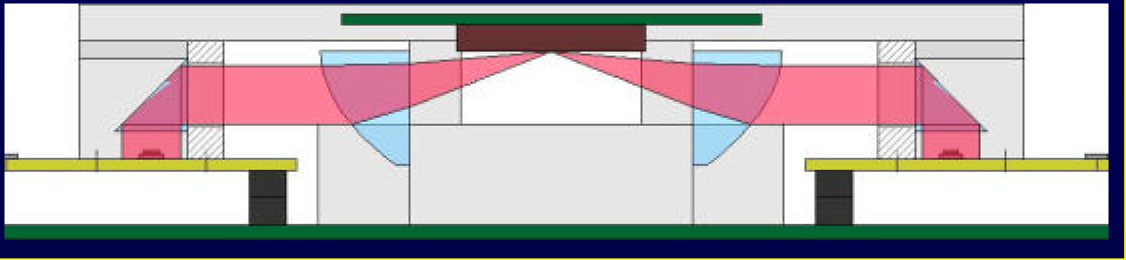
- Uniformity and reliability of o/e components
  - – Need to build fancy power hungry receivers ***or***
  - – Add ecc into communications link



- Thermal expansion affects optical path
  - – Need physically symmetric architecture



- Packaging and Free Space Optics “Hard”
  - – Use guided wave optics integrated with packaging



Estimation, Simulation, “Error Bars”

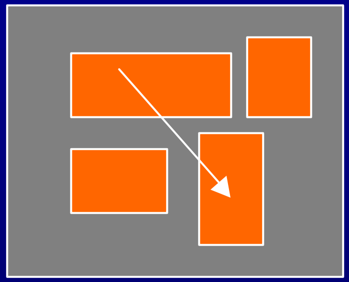
- How good is the answer?
- How good does it have to be?

HW/SW

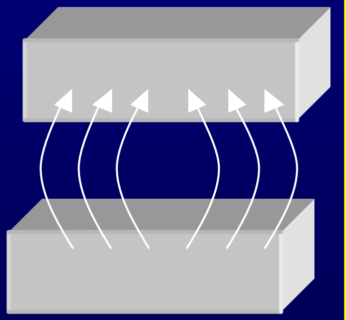
New(obj2)

Functional

After 10 ns



RTL



Layout

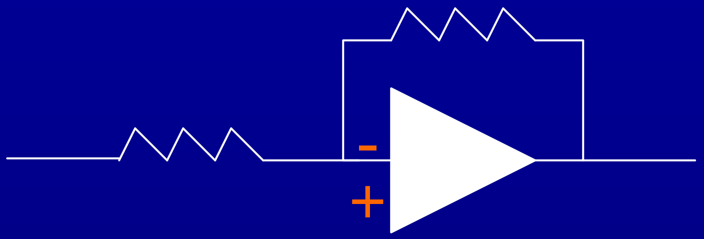
Physics

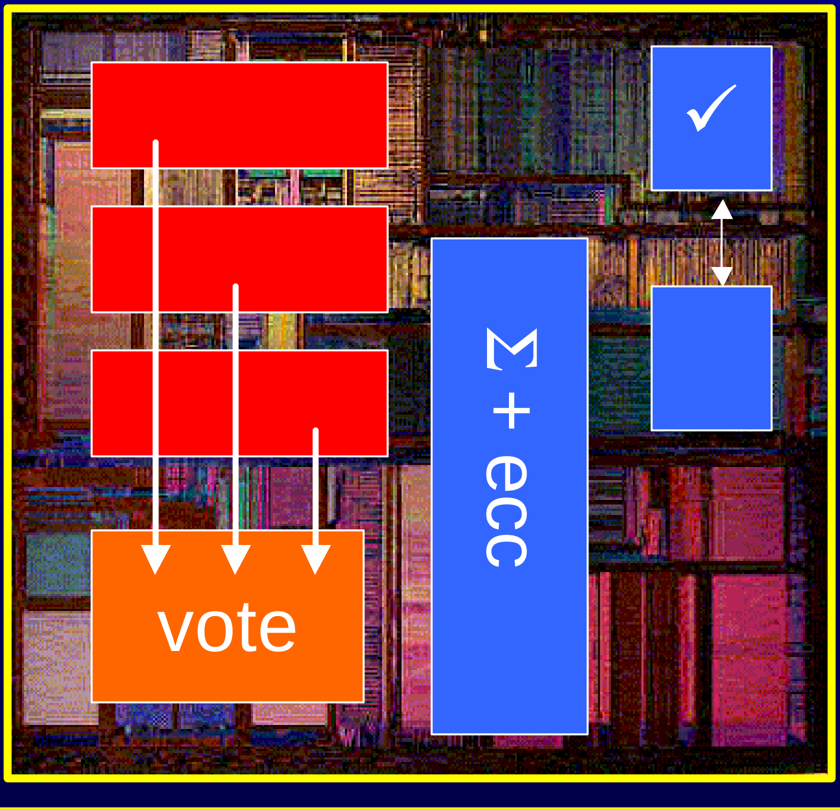
Validation Choices:

- Co-simulation
- More detailed models at higher levels
- Reduced order models
- Hardware emulation
- Physical prototyping

Use architectural solutions for technology problems

- Use the real-estate
- Reliability:
  - Redundancy
  - Integral error correction
  - Fault tolerance
  - Self-repair
- Integrated CAD tools for error and reliability modeling
  - trade off noise margins for error codes





Manufacturing & packaging are the solution, not the problem

- Multi-domain architectural solutions are the answer to mixed technology packaging problems
  - Self aligned MOS gate
  - Inductance of power pins help the power supply
  - Use insulating diamond substrate for heat removal
  - Use rigid fiber bundles for integrated optics

Conclusions

- Need better verification tools
  - Both multi-level and multi-domain
  - Both estimation and simulation
  - Both results and tolerances
- Need reliability aware tools
  - Fault modeling, fault tolerant synthesis
- Need architecture based tools
  - Mixed technology trade-offs
  - "Outside the box"

James D. Murphy

Program Manager

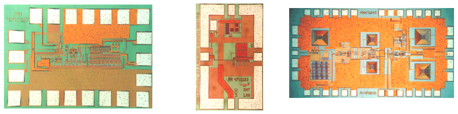
Microsystems Technology Office

(703) 696-2250
jmurphy@darpa.mil

Mixed Signal System on Chip

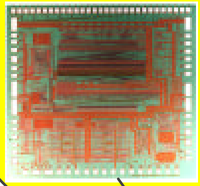
RF/Analog Processing

LNA, Mixer, PLL, Video Processing, LogAmp,



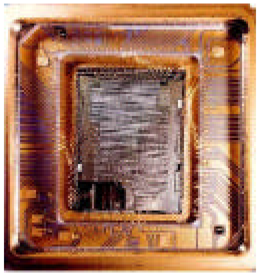
Data Conversion

A/D, AC, ΔΣ



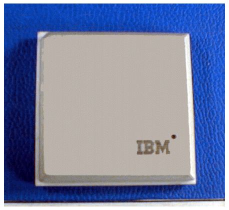
High Speed Digital

DDS, Mux, DeMux, High Speed FIR, IIR

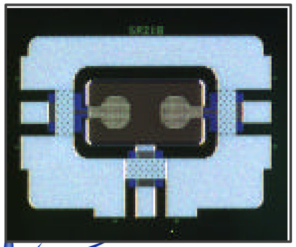


High Gate Count CMOS

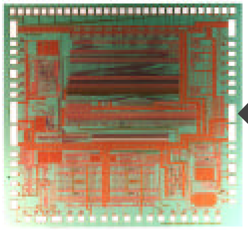
Digital Processing, Tuner, FIR, IIR, FFT, T&C, Control



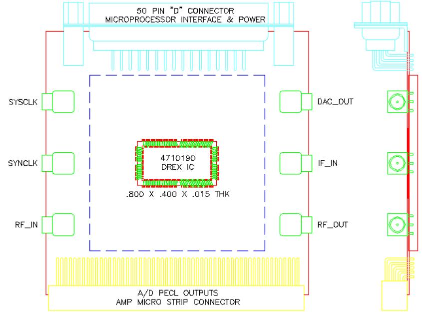
Post Processing



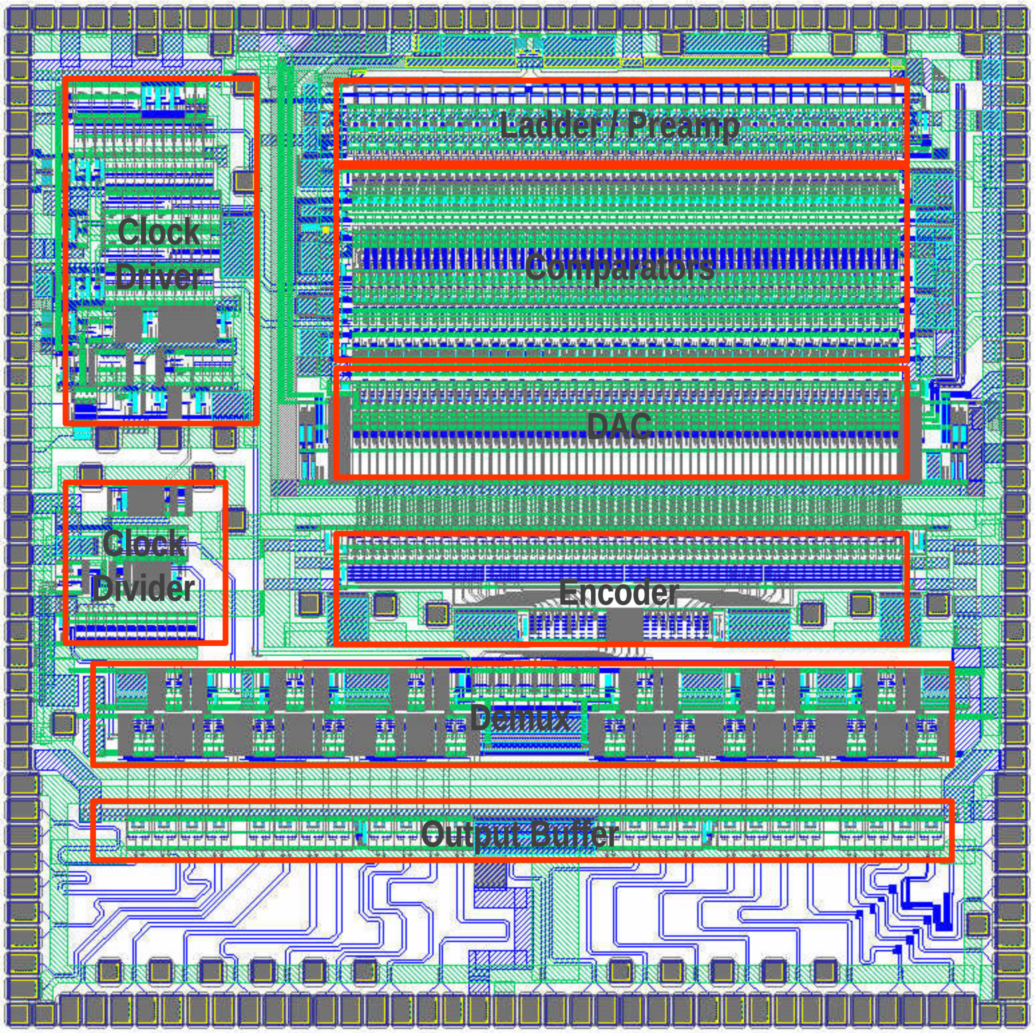
MEMS TopSide



Packaging

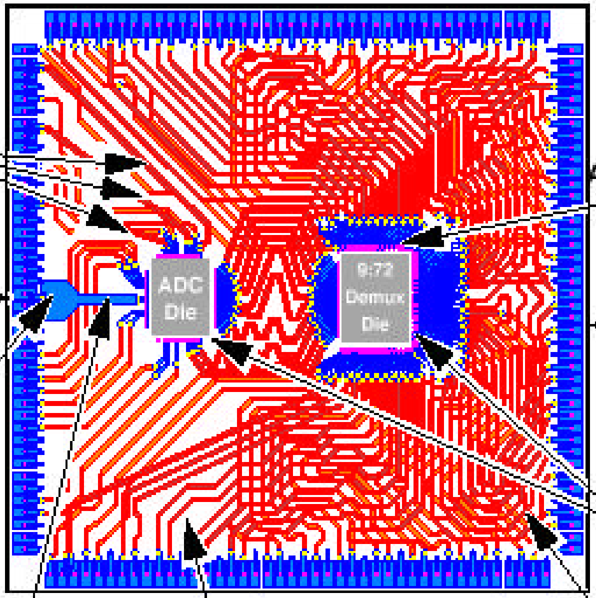


Advanced Digital Receiver ADC/DAC - Demux



- 6 bit ADC
- 6 bit DAC
- 3.2 GS/s Clock
- 1:4 Output Demux
- DAC thermal noise 1 nV/√Hz
- DAC full scale 3V

Advanced Packaging Requirements for Digital Receivers



Ultra-Wideband Digital Signal Interconnects for Clock Lines and ADC to Multiplexer Must Not Degrade ~ 30 ps Risetimes Controlled Z_o and Propagation Velocity to Avoid Skew

Differential Analog Signal Inputs with Multi-GHz Bandwidths

Precision Differential Input Signal Lines:
- -Low Loss Up to Microwave Frequencies
- -Very Tight Z_o Control for Low Signal Reflections (VSWR)
- -Even/Odd Mode Matching for Differential Inputs

Precision, Small-Size 50 Ω Embedded Termination Resistors Accurately Terminate Digital Interconnects (Low VSWR)

Small MCM Layout Size for Compact Layouts/Minimal Reflections

Flip-Chip Die Attach for Very Low Discontinuities (Parasitic Bond Inductances) at Chip I/O's

ABSOLUTELY CRITICAL That Crosstalk from Digital Outputs Back to Analog Inputs be Essentially Zero (<< 1 mV Differential) to Preserve Spur-Free Dynamic Range of A/D

Power/Ground Planes Must be Very Low Resistance and Inductance with Embedded High C/A Layer to Avoid Crosstalk Through Power Supplies (Multiple Supplies Often Required)

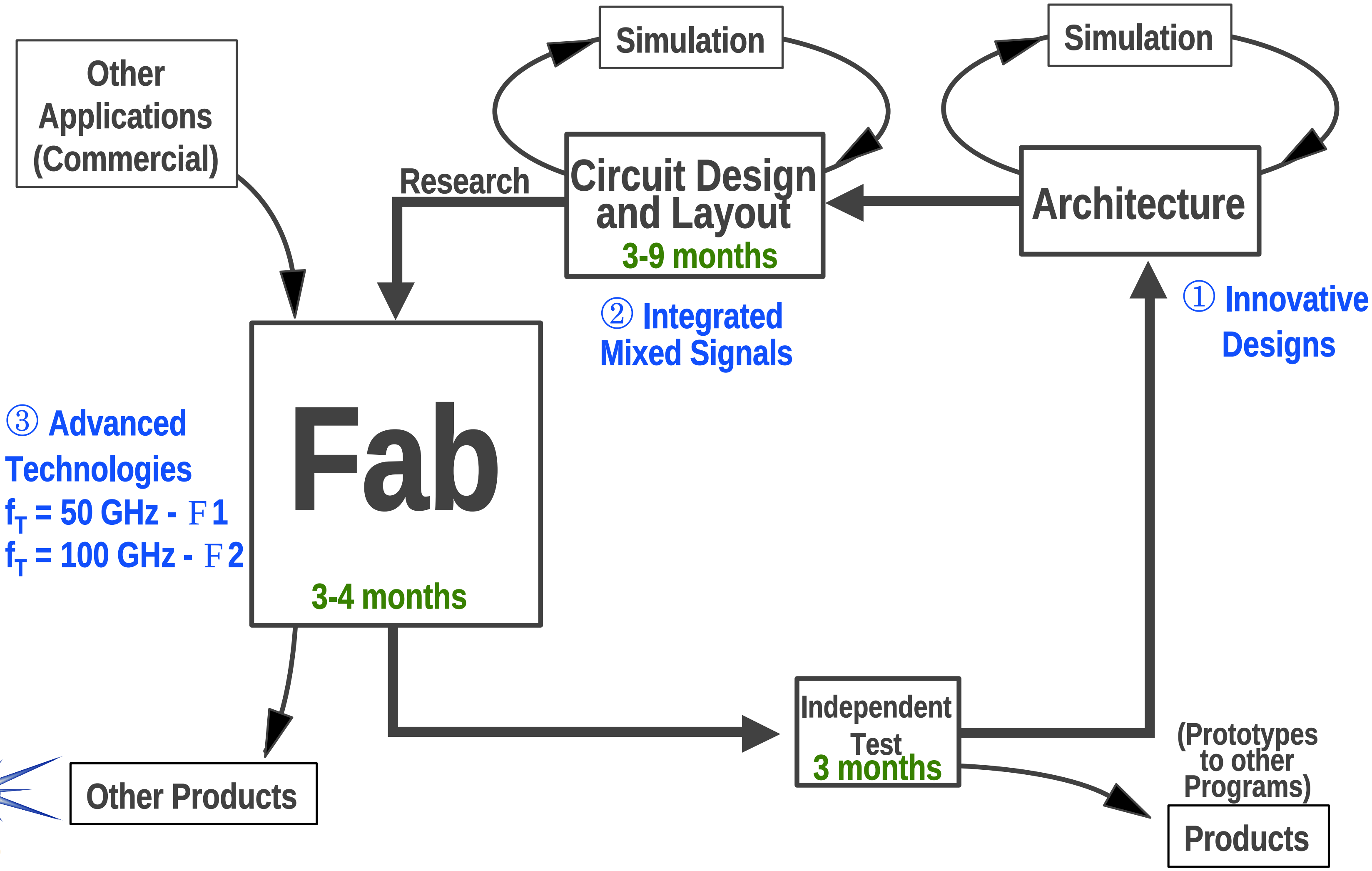
High Density Fine-Pitch MCM Interconnect Layers for "Normal" Digital Signals

ADC = A/D Converter
C/A = Capacitance/Area
MCM = Multichip Module

Mux = Multiplexer
Demux = Demultiplexer
Z_o = Transmission Line Impedance

I/O = Input/Output Leads
VSWR = Voltage Standing Wave Ratio

High Performance A/D Converter Development Cycle



Simulation

Simulation

Other Applications (Commercial)

Research

Circuit Design and Layout
3-9 months

Architecture

① Innovative Designs

② Integrated Mixed Signals

③ Advanced Technologies
f_T = 50 GHz - F1
f_T = 100 GHz - F2

Fab
3-4 months

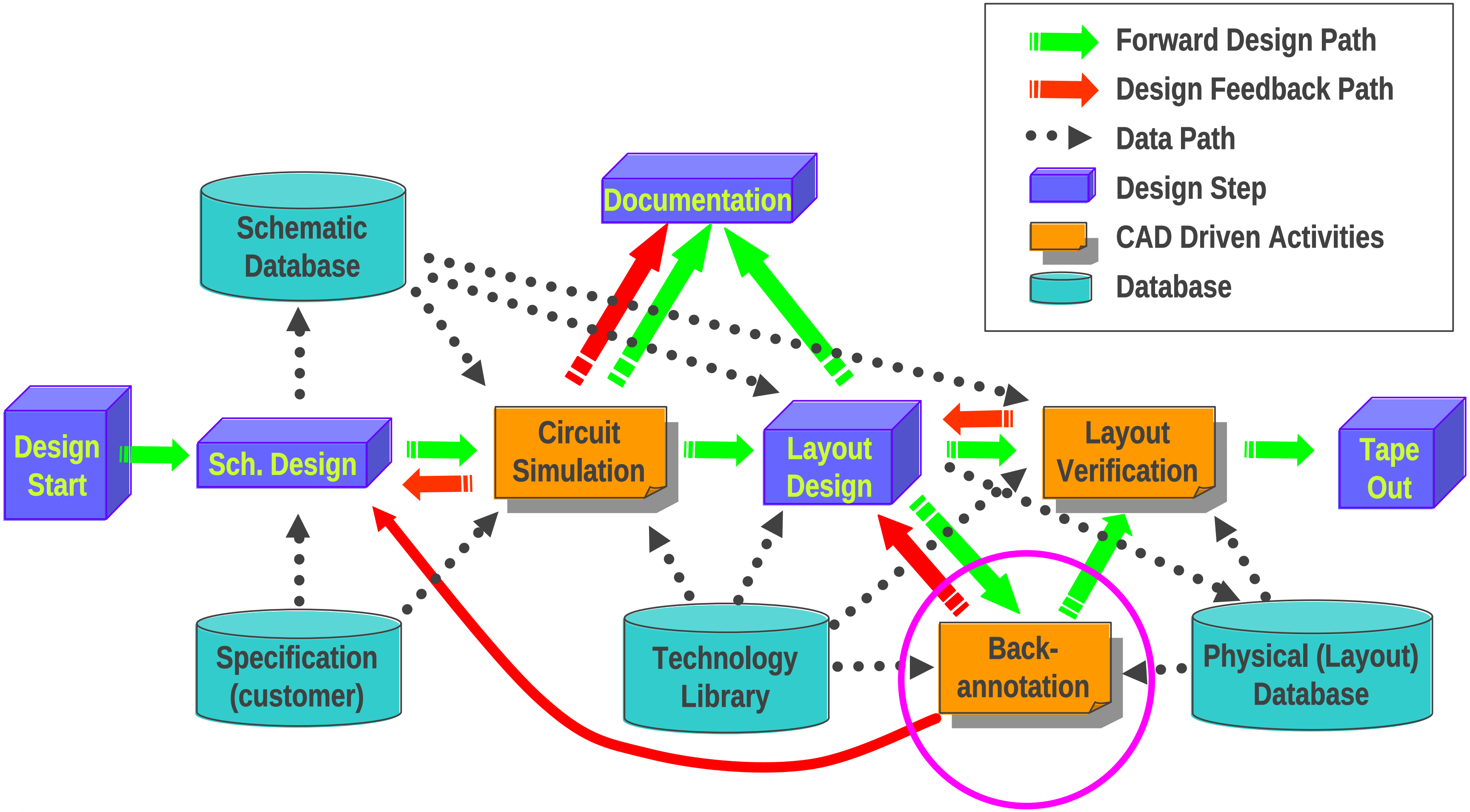
Independent Test
3 months

(Prototypes to other Programs)

Other Products

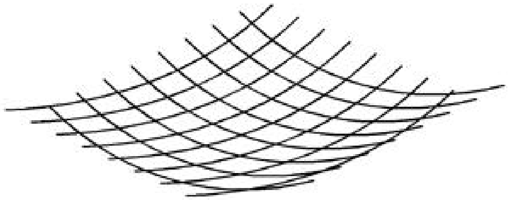
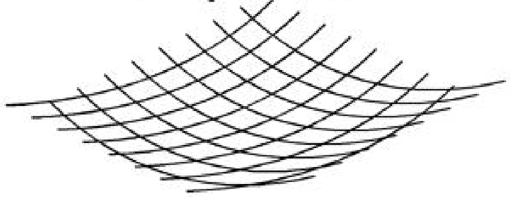
Products

Design Methodology

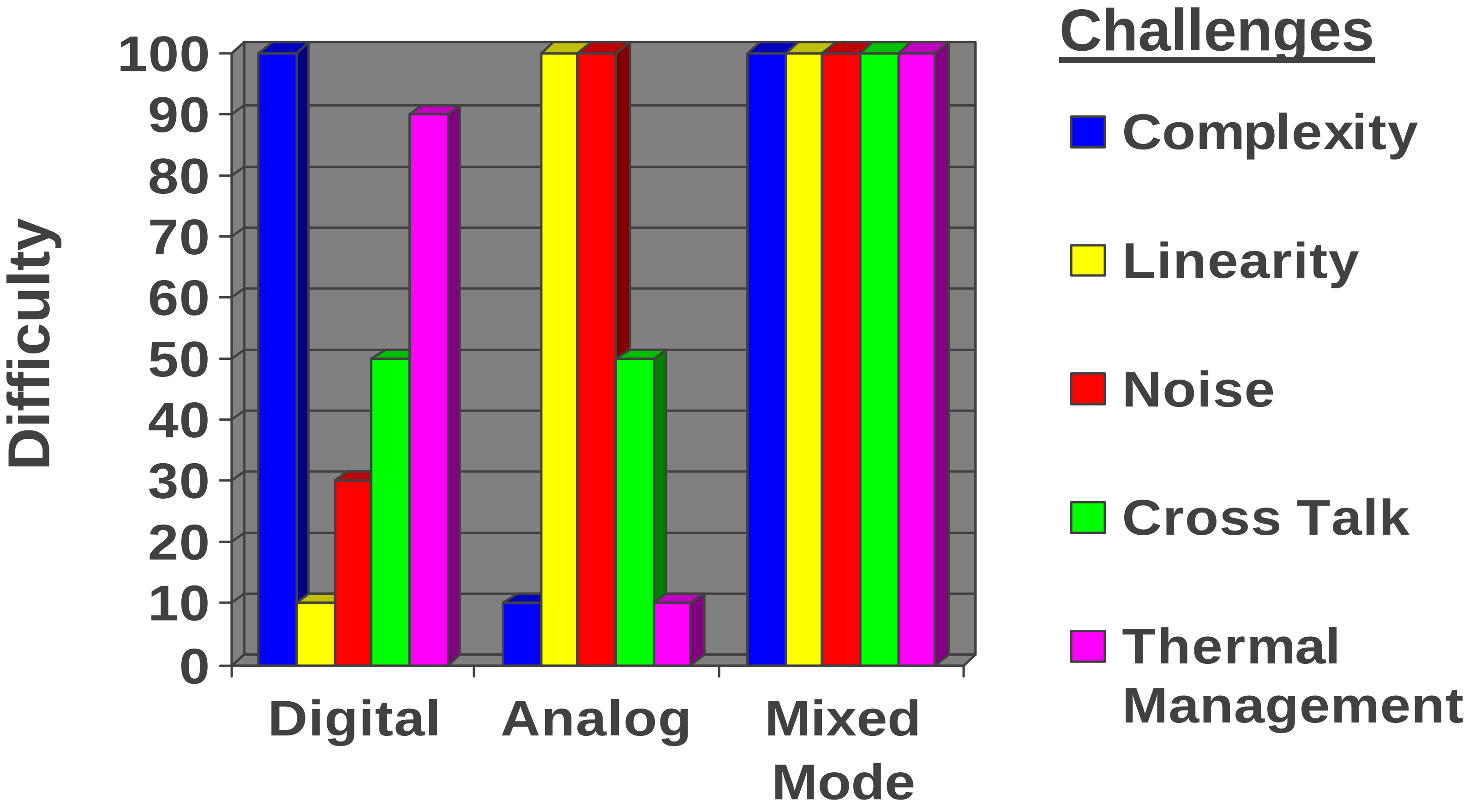


Weakest point in design cycle. Hard to automate, involves manual work, intuition and use of non-integrated electromagnetic simulation tools (BIG problem for high speed mixed signal IC)

The Mixed - Signal Design Problem

Type of Circuit	**Microprocessors Digital Circuits**	**Analog-Digital Converters**	**RF/Microwave Linear Circuits**
Millstones (Key Problem Areas)	**Extreme Complexity** ($\approx 10^8$ Transistors) **High Clock Rates** ($f_c \approx$ 500MHz-1GHz) **Large I/O Counts** (Severe SSON)	**Extreme Wideband Crosstalk Sensitivity** **Very High Clock Rates** ($f_c \approx$ 1GHz - 5+GHz) **High Internal ac Gains** **High Complexity** ($\approx 10^4$ Transistors)	**Extremely High Signal Frequencies** ($f_{sig} \approx$ 100MHz-100GHz) **Very Low Noise** **Very High Linearity** **Complex E&M**
		**No Safety Net!**	
Saving Graces (Why Designs Usually Work)	**High Noise Margin** (Crosstalk Tolerance) **Saturated Operation** (No ac Gain Most of Time) **Excellent LVS CAD Tools (Overlap Cap Extraction)** **Package E&M Modeling** (Model SSON Solutions)	Complex circuits with severe internal (on-chip) E&M issues, causing oscillations, loss of performance. Full-wave E&M solvers far too slow; need fringe capacitance, self and mutual inductances in distributed interconnect models back-annotated into circuit simulations.	**Narrowband Operation** (Eases Stability & Distortion) **Circuit Simplicity** ($\approx$1-100 Transistors) **E&M Solvers Applicable** (Due to Simplicity) **Hand Tuning and Fast "Cut & Try" Circuit Board Turnaround**

The Mixed Signal Design Challenge



Source: B. Jalali, UCLA

MIXED TECHNOLOGY SYSTEM ON CHIP

CAD DESIGN REQUIREMENTS

AFRL/IFTC
Robert G. Hillman

Robert.Hillman@afrl.af.mil
(315) 330-4961

INFORMATION DIRECTORATE

W - Wright Site

R - Rome Site

(R) (315) 330-xxxx
(W) (937) 255-xxxx + ext
(R) DSN 587-xxxx
(W) DSN 785-xxxx

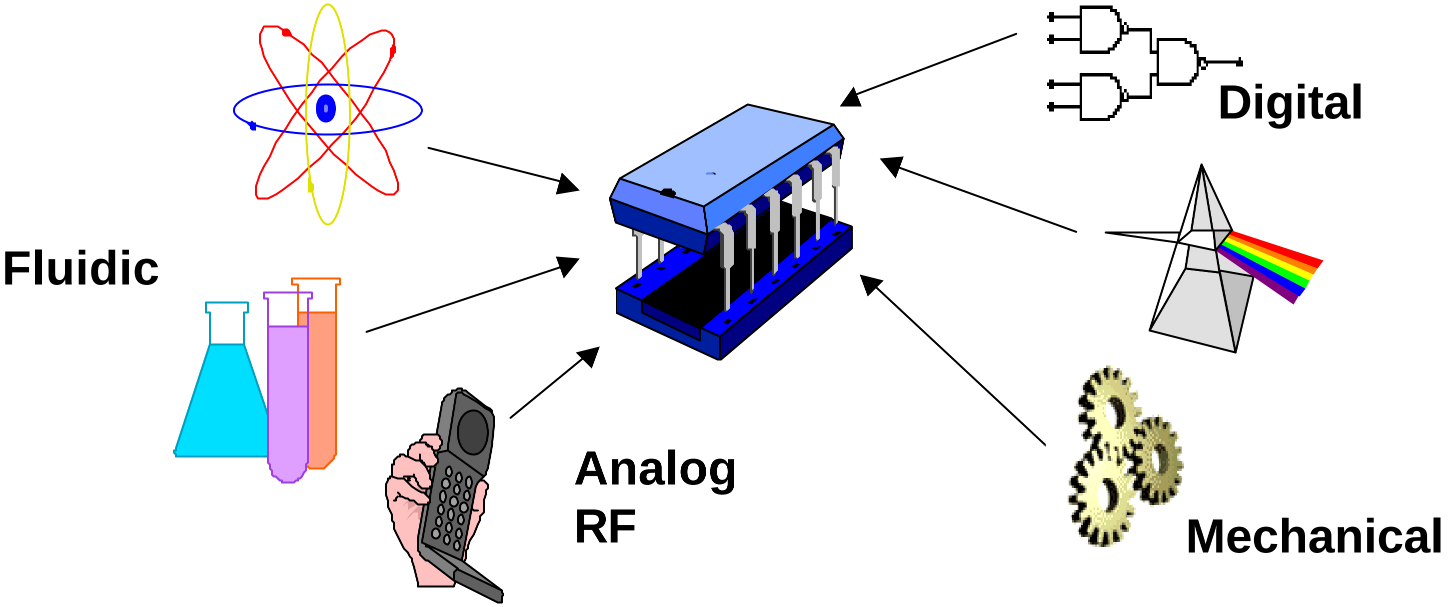
INFORMATION DIRECTORATE
IF x7701
Raymond Urtz, Director
Col John Bedford, Dep Director
John Graniero, Chief Scientist

- BUSINESS MGMT
IFB x7052
Jack Mineo, Acting Chief
- CONTRACTING
IFK x 4739
Lt Col Ralph Lentz, Chief
- FINANCIAL MGMT
IFF x3507
Jean Iselo, Comptroller
- CORPORATE INFORMATION
IFI x1714
Lt Col Frederick Berg Chief
- SITE OPS
IFO x4321
Dan Bollana, Acting Chief
- STRATEGIC PLANS
IFR x2041
Igor Plonisch
Dr John Hines (W)

- INFORMATION TECHNOLOGY DIVISION
(IFT) x3011
Eugene Blackburn, Chief
Dr Northrup Fowler, Tech Adv
  - W EMBEDDED INFORMATION SYSTEMS ENGINEERING (IFTA)
  - R DYNAMIC COMMAND & CONTROL (IFTB)
  - R ADVANCED COMPUTING ARCHITECTURES (IFTC)
  - R INTELLIGENT INFORMATION SYSTEMS (IFTD)
- INFORMATION GRID DIVISION
(IFG) x2165
Daniel McAuliffe, Chief
Carmen Luvera, Dep Chief
Dr Warren Debany, Tech Adv
  - R DISTRIBUTED INFORMATION SYSTEMS (IFGA)
  - R DEFENSIVE INFORMATION WARFARE (IFGB)
  - R INFORMATION CONNECTIVITY (IFGC)
  - W PLATFORM CONNECTIVITY (IFGD)
- INFORMATION & INTELLIGENCE EXPLOITATION DIVISION
(IFE) x2976
Joseph Camera, Chief
John McNamara, Tech Adv
  - R FUSION TECHNOLOGY (IFEA)
  - R INFORMATION HANDLING (IFEB)
  - R MULTI-SENSOR EXPLOITATION (IFEC)
  - R GLOBAL INFORMATION BASE (IFED)
- INFORMATION SYSTEMS DIVISION
(IFS) x4175
James Cusack, Chief
Dr. Heather Dussault, Tech Adv
  - R SYSTEM CONCEPTS & APPLICATIONS (IFSA)
  - R C4ISR MODELING & SIMULATION (IFSB)
  - W ADVANCED ARCHITECTURE & INTEGRATION (IFSC)
  - W COLLABORATIVE SIMULATION TECHNOLOGY & APPLICATIONS (IFSD)
  - R SYSTEM DEMONSTRATION AND INTEGRATION (IFSE)

MIXED DOMAIN INFORMATION SYSTEMS

- **Merging Functional Elements**
  Sense, Compute, Actuate, and Communicate



Fluidic

Digital

Analog
RF

Mechanical

- **Single Silicon Substrate**
  - Monolithic or Minimally assembled
  - Sub-micron to 100s of microns in scale

PARADIGM SHIFT
DEFINITION OF ULTRA SMALL SYSTEMS

- **Target Metrics**

Performance	5x-1000x increase
Power Consumption	5x-1000x decrease
Parts Count	10x-100x decrease
Size	10x-10000x decrease
Cost	10x-100x decrease

- **Revolutionary Advancements in Military Systems**

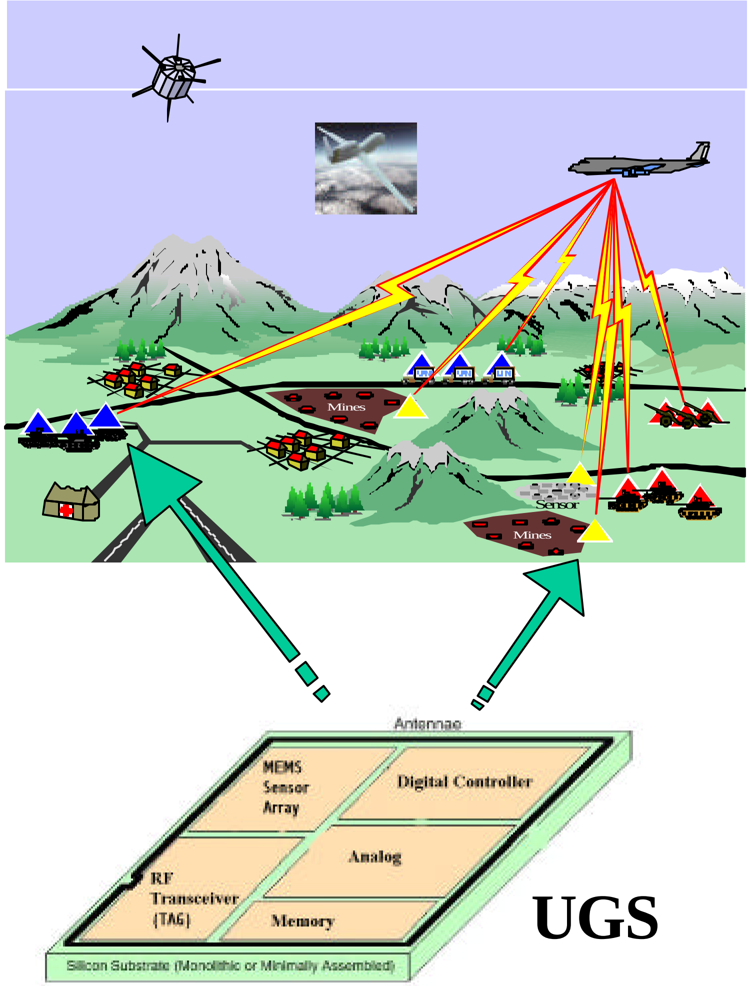
  - Wireless Communications
  - Satellite Communications
  - Smart Munitions
  - Radar
  - Electronic Countermeasures
  - Unmanned Air Vehicles
  - Inertial Navigation
  - Telemedicine

Microelectromechanical Systems for C2ISR Applications

Problem: The need to reduce the size, weight, and power of autonomous information nodes that provide real-time data for exploitation and dissemination, and provide ID location of friendly assets for Battlefield Awareness.

Approach: Exploit MicroElectroMechanical Systems (MEMS) technology to allow affordable, fault tolerant, low power, ultra-small information nodes that integrate arrays of sensors (video, seismic, electromagnetic, acoustic, environmental & BW/CW), advanced on-board processing, mass digital data storage, and wireless communications.

Uniqueness: AFRL - Rome Research Site is the AF lead in advanced information processing, and MEMS design. Possess in-house facilities to design, test, and prototype an Integrated Micro-Information System.



Users: Micro-UAVs, Nanosatellites, Unattended Ground Sensors (UGS), & RF Tags

Systems-on-a-Chip Design

Bob Brodersen
Dept. of EECS
Univ. of Calif.
Berkeley

http://bwrc.eecs.berkeley.edu

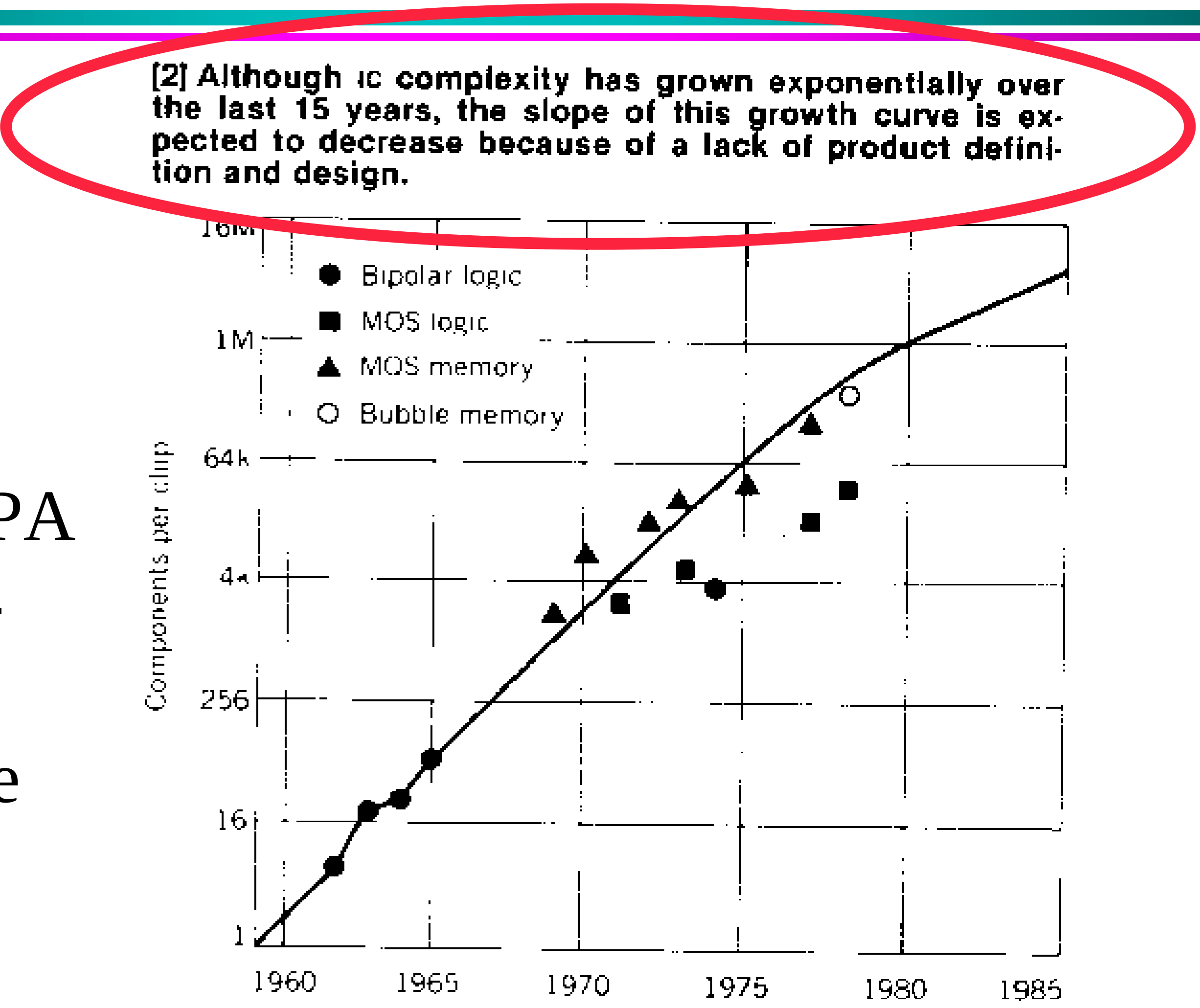
The Misuse of CMOS

- The limitations of CMOS is the definition of applications and their design, not due to the technology – *we don't need new devices, we just need to learn how to use CMOS*
- CMOS is vastly underutilized
  - » Wrong architectures for the technology
  - » Inadequate design methodologies
  - » Too long and risky implementation paths
  - » Historical inertia

Moore’s Law (the original)

Not a new problem

Last time it happened DARPA help solve it - The VLSI program of the 1980’s



[2] Although IC complexity has grown exponentially over the last 15 years, the slope of this growth curve is expected to decrease because of a lack of product definition and design.

Goden Moore, IEEE Spectrum 1979

Increasing Use of Software is a Key Problem

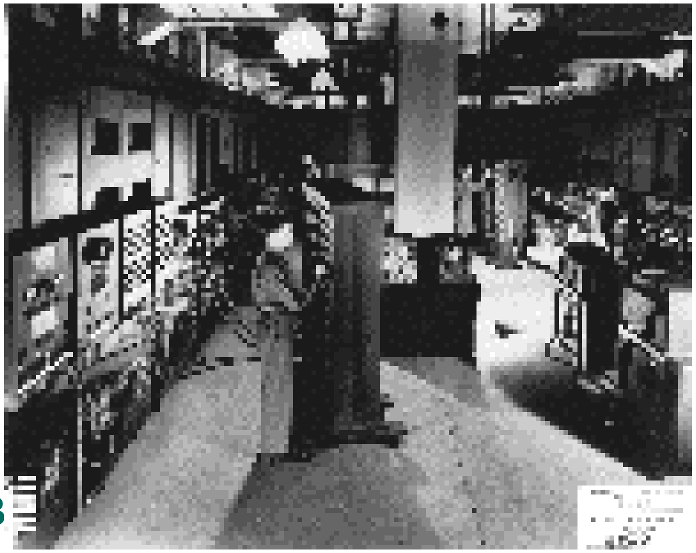
- Incredibly inefficient and getting worse (losing factors of 100-10,000 in area and power)
- Unverifiable – solution has been to expect and to live with “bugs”, crashes, patches…
- Not the best (or even a good) description for most embedded applications
- The success of software for general purpose computing does not apply to embedded systems

What is the problem?

The Von Neumann architecture was developed in 1945!!

The assumptions back then

- Hardware is expensive
- Scientific computation is the application
- Cost, size and power are not an issue
- Hardware and software were separate



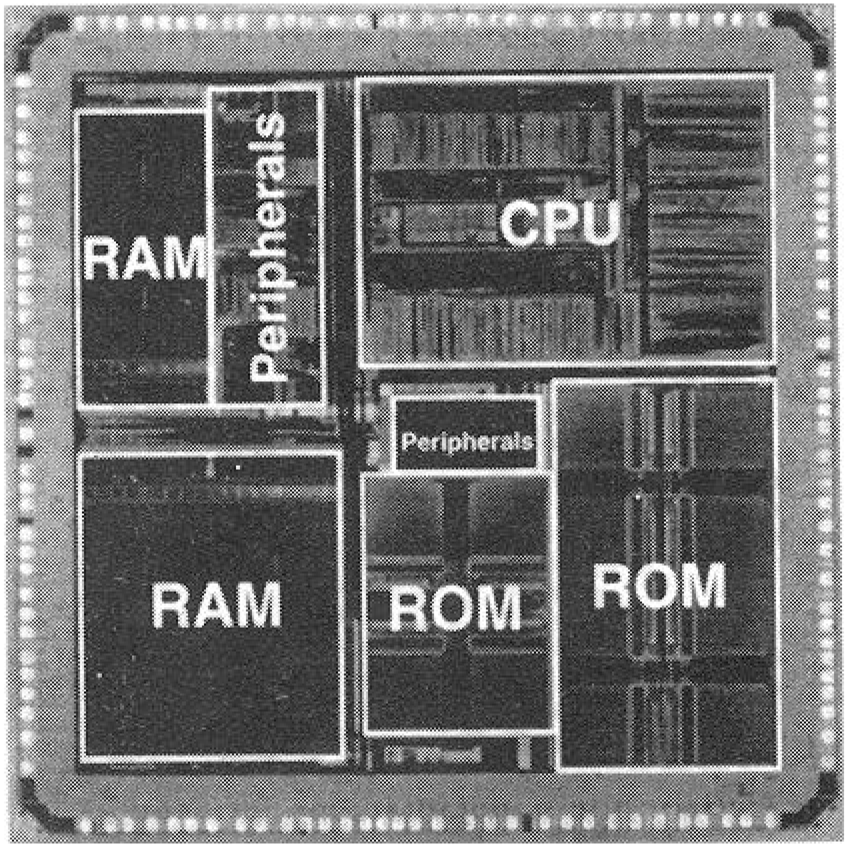
Time sharing the
hardware
was absolutely necessary

The Situation Now for Embedded Applications

- Hardware is cheap
  - Potentially 1000’s of multipliers on a chip
- Power, cost and size is critical
- Applications are I/O and DSP intensive
- Software is becoming “harder” than hardware
- Hardware and software are on one chip

Time multiplexing … Why do it?

DSP processor
(25 mm^2)



12x12 multiplier
(.05 mm^2)

Approach for SOC Design

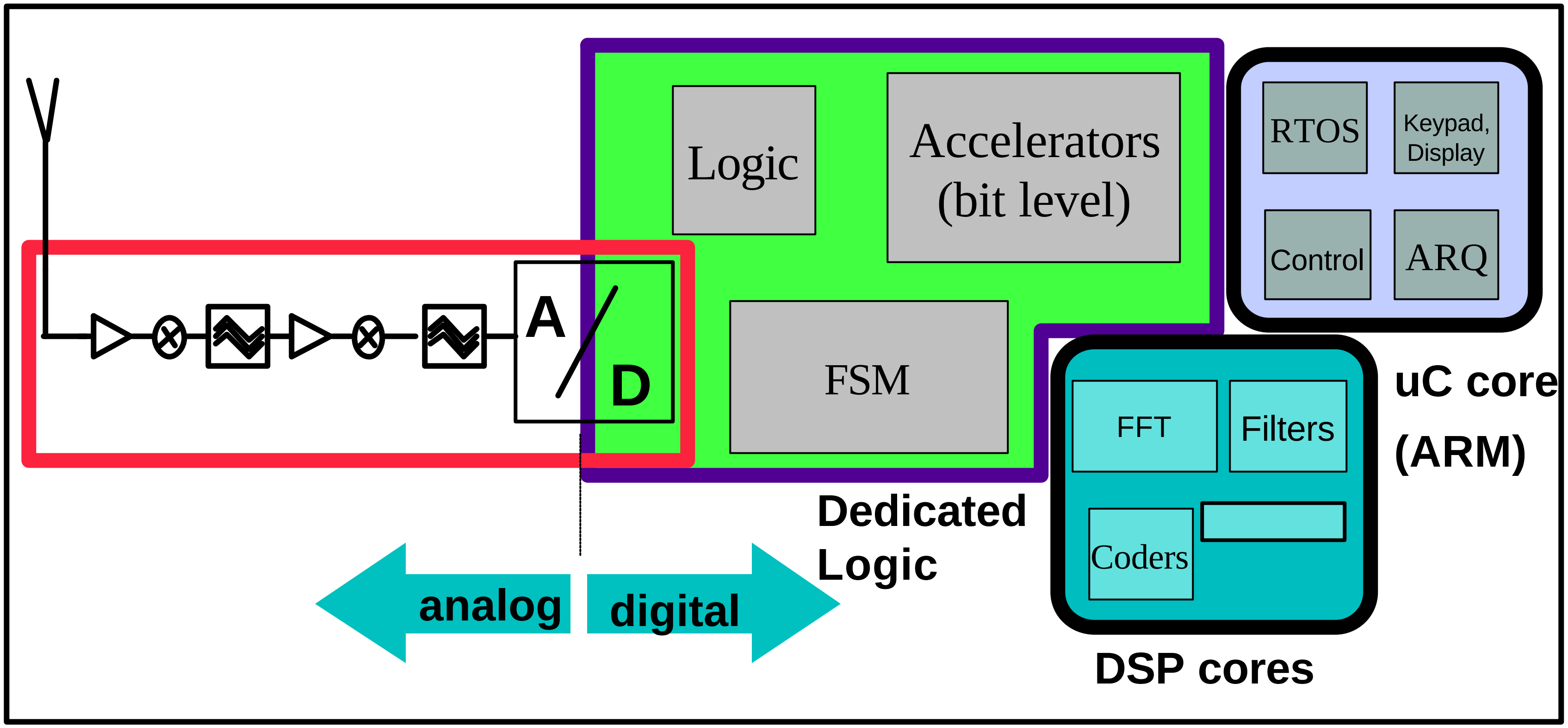
- Domain specific system design
  - Optimized performance, area and power architectures
  - Optimized design tools and descriptions
- Reduction of design time
  - Minimize system description re-entry
  - Rapid implementation – designs of chip in a day from algorithm/application description
  - Incorporate analog design
  - Automate verification

First Choose a Domain

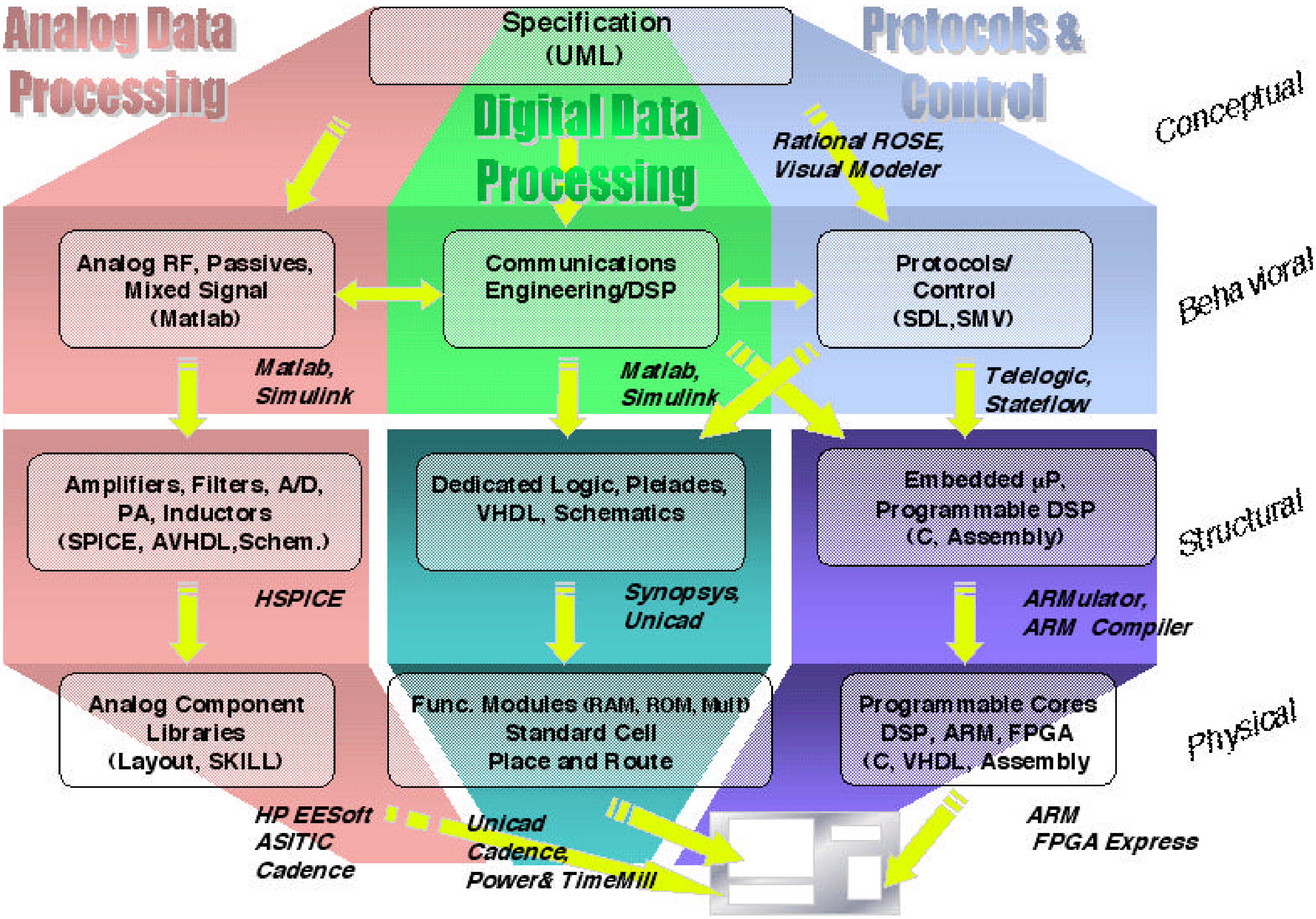
Analog Baseband and RF Circuits

Communication Algorithms

Protocols



Next define the Complete System Design Environment



Specification
(UML)

Analog Data Processing

Digital Data Processing

Protocols & Control

Conceptual

Rational ROSE,
Visual Modeler

Analog RF, Passives,
Mixed Signal
(Matlab)

Communications
Engineering/DSP

Protocols/
Control
(SDL,SMV)

Behavioral

Matlab,
Simulink

Matlab,
Simulink

Telelogic,
Stateflow

Amplifiers, Filters, A/D,
PA, Inductors
(SPICE, AVHDL,Schem.)

Dedicated Logic, Pleiades,
VHDL, Schematics

Embedded μP,
Programmable DSP
(C, Assembly)

Structural

HSPICE

Synopsys,
Unicad

ARMulator,
ARM Compiler

Analog Component
Libraries
(Layout, SKILL)

Func. Modules (RAM, ROM, Mult)
Standard Cell
Place and Route

Programmable Cores
DSP, ARM, FPGA
(C, VHDL, Assembly)

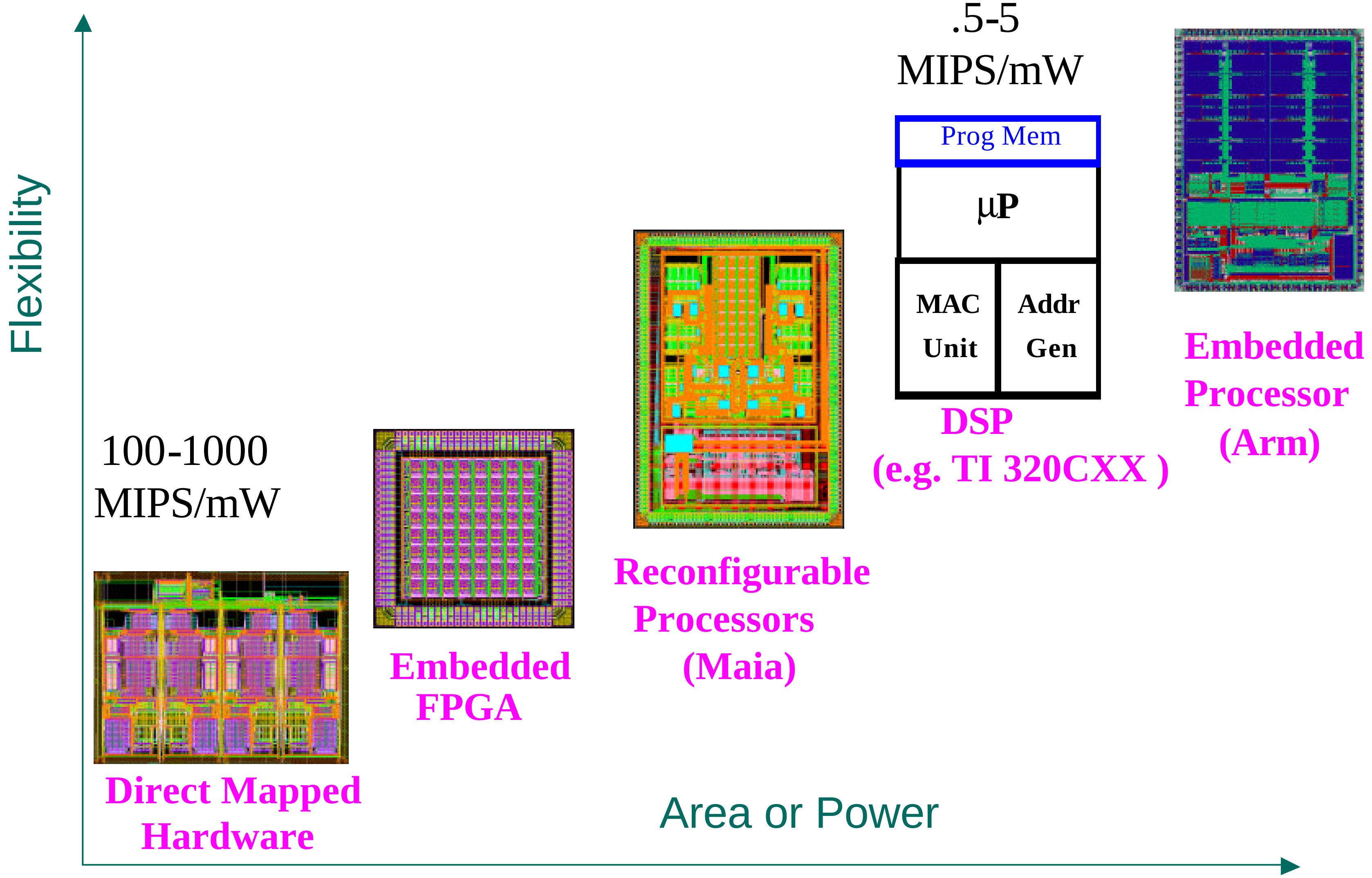
Physical

HP EESoft
ASITIC
Cadence

Unicad
Cadence,
Power& TimeMill

ARM
FPGA Express

Then choose the right architectures …



Flexibility

100-1000 MIPS/mW

Direct Mapped Hardware

Embedded FPGA

Reconfigurable Processors (Maia)

.5-5 MIPS/mW

Prog Mem

μP

MAC Unit

Addr Gen

DSP (e.g. TI 320CXX)

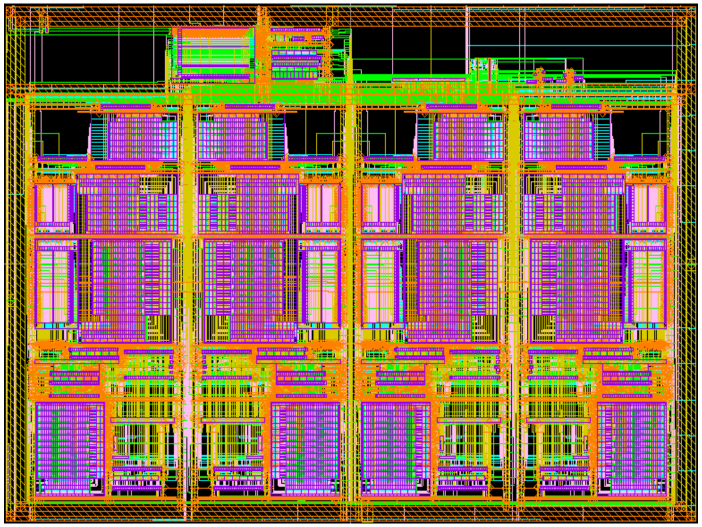
Embedded Processor (Arm)

Area or Power

Then get technology access…

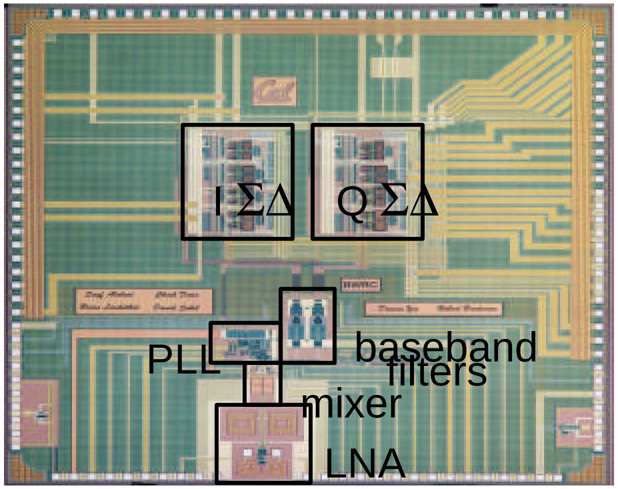
- Probably the only advanced country in the world that doesn't have subsidized CMOS access
- Look what happened
  - Tool development in the physical design essentially stopped
  - One dominant commercial flow emerged which is now beginning to fail
  - No community of designers and CAD developers to determine if advances are being made

Do experiments and learn from the results

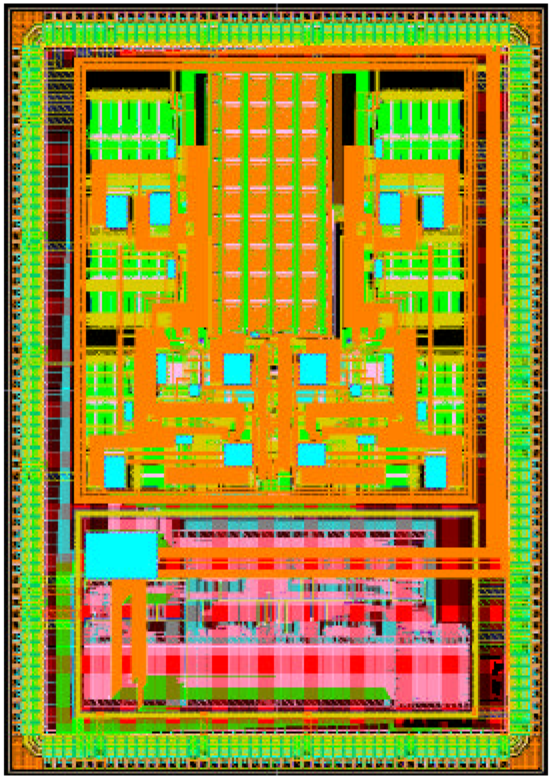


Direct map
Multiuser detection
200 MIPS/mW

100 mW Direct conversion
2 GHz CMOS RF



Reconfigurable interconnect
5-10 MIPS/mW



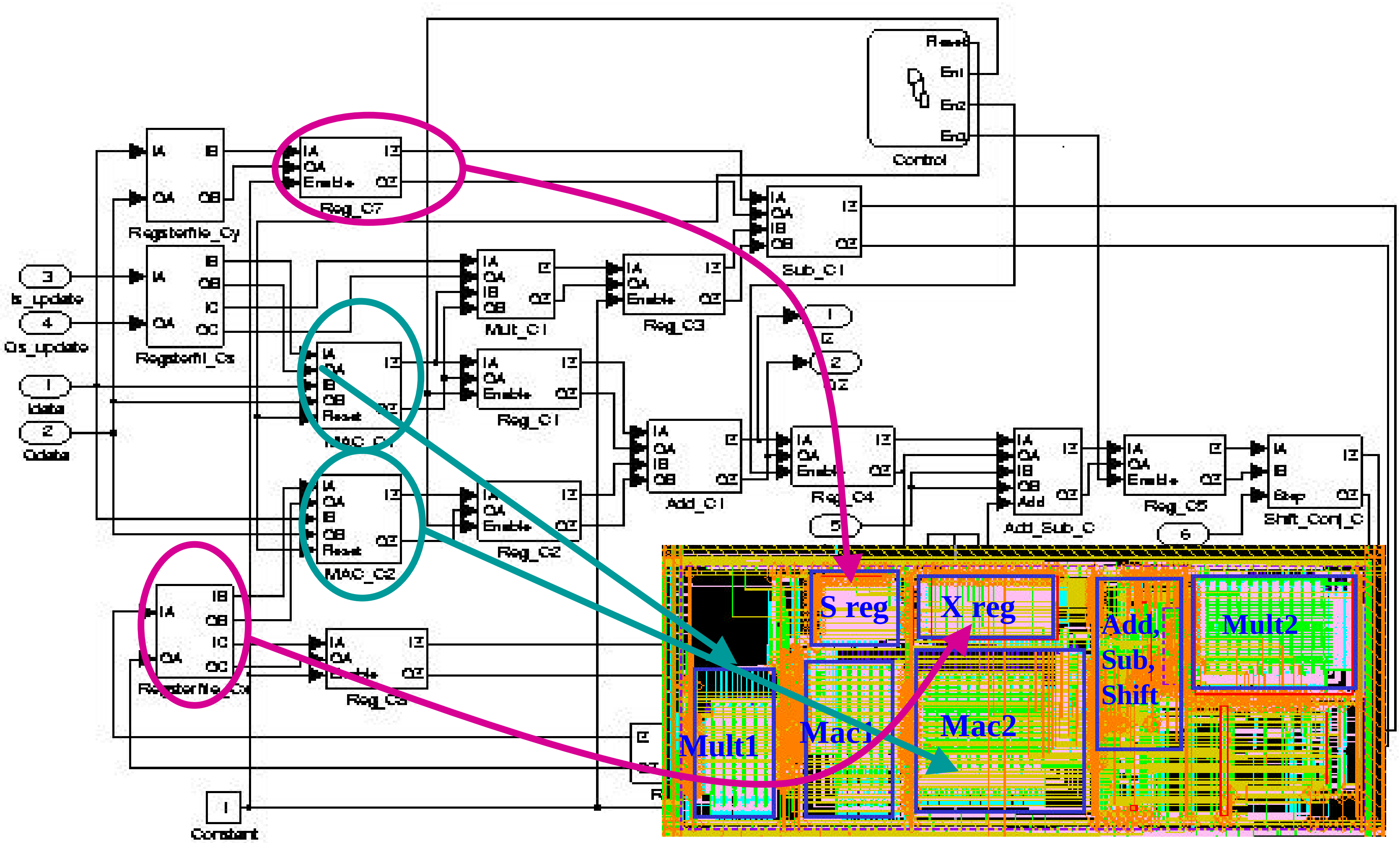
Generalizing the approach

- Need an infrastructure that can be reused for different domains
- Define common tools and sharing the support
  - Commercial tools
  - Modeling
  - Libraries
- Common strategy for technology access

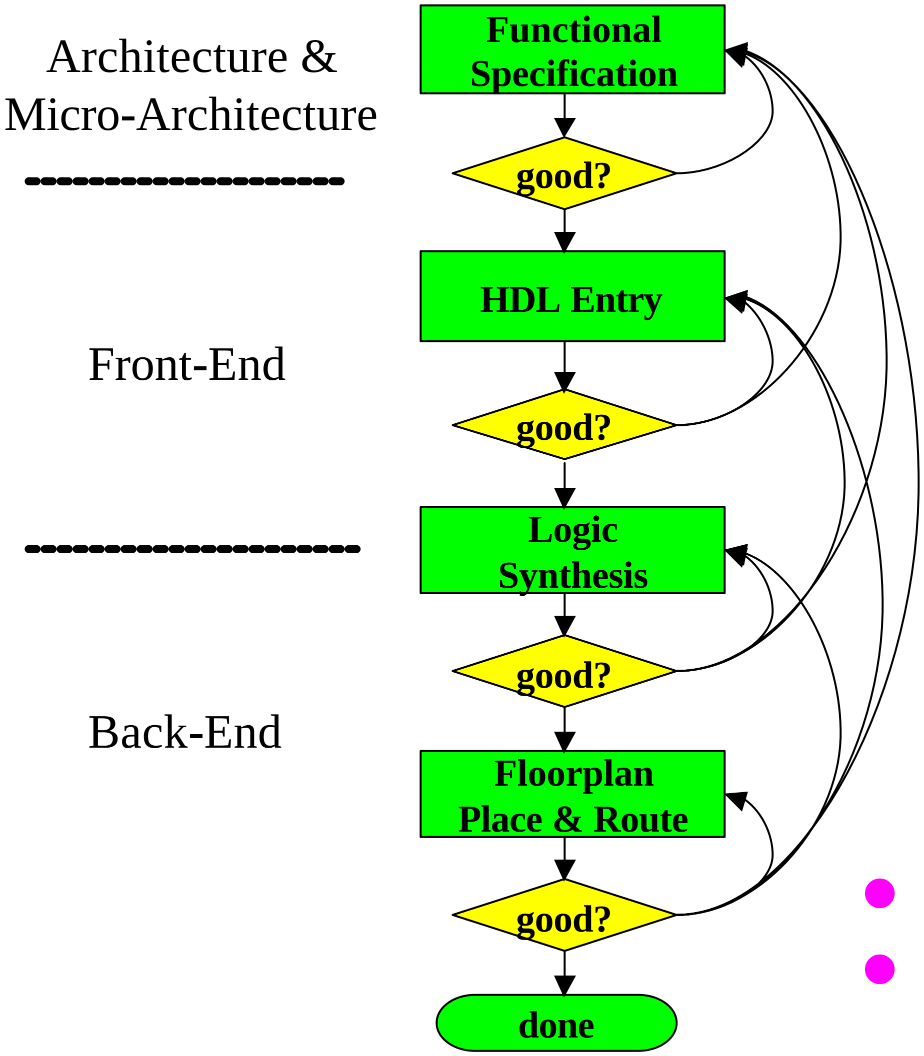
More Specifically

- Direct map design approach
- Energy efficiency of optimized CMOS architectures
- RF CMOS capabilities

Mapping the Algorithm into Hardware



How to do this design?


Architecture &
Micro-Architecture

Front-End

Back-End

Functional Specification
good?
HDL Entry
good?
Logic Synthesis
good?
Floorplan Place & Route
good?
done

Standard design flow????

Difficulties:

- Logic Verification
- Timing Closure
- Routing Congestion

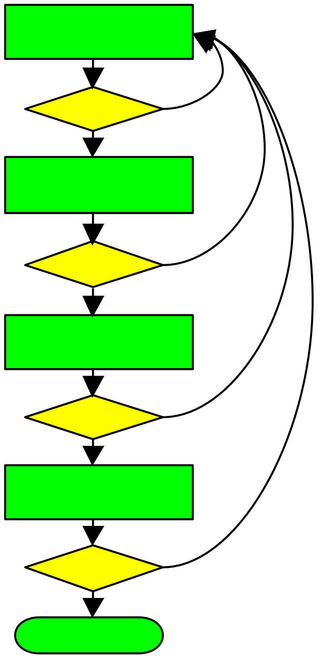
Critical Problem:

Indeterminate Design Time

- Design Decisions made at Every Step
- Critical information lost below Architecture level

What is needed

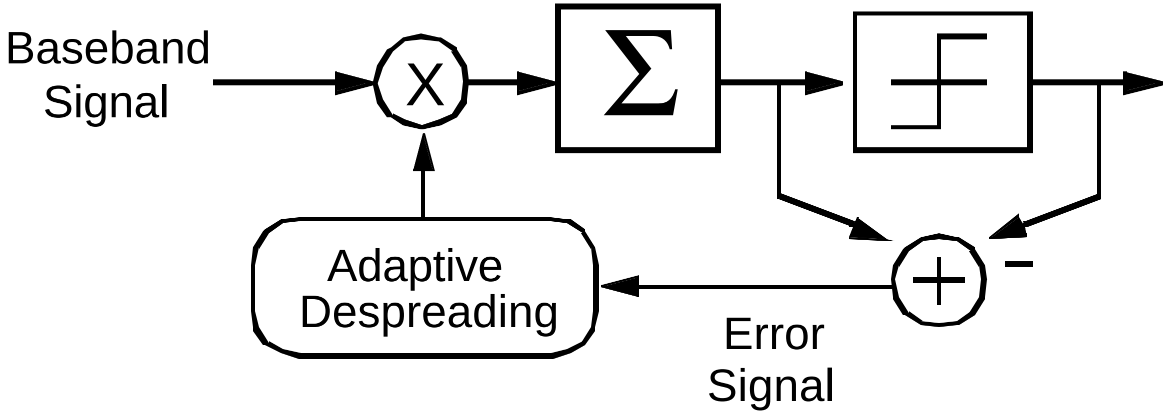
- Full Automation
- Make design decisions at top level
- Support for multiple architectures



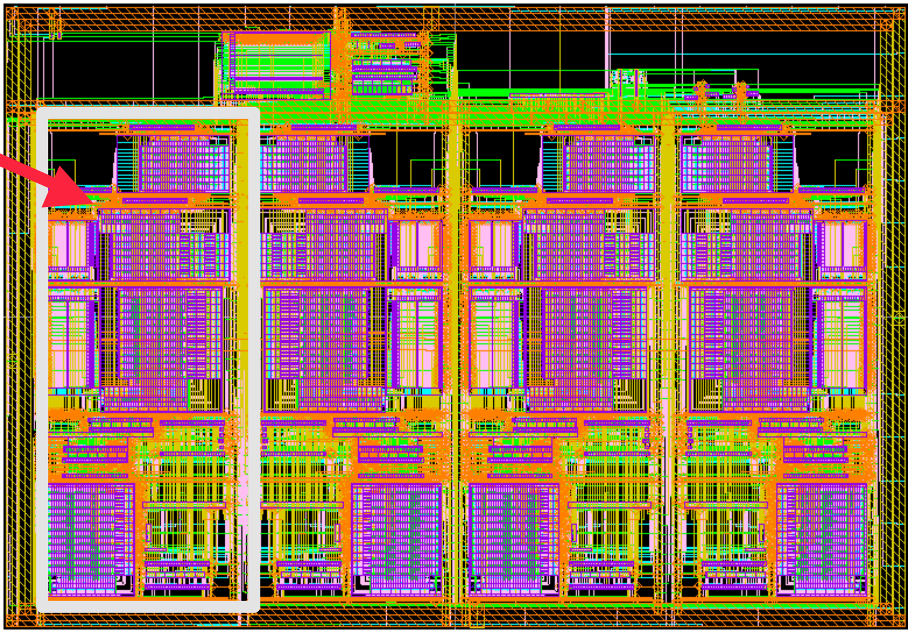
Goal:

Provide predictability in the design process

Fully parallel implementations



- *Basic building block - adaptive correlator*
- *25 MHz clock*
- *36 multipliers*
- *1.2 GOPS (operations = multiplies,adds and MAC's)*



Comparison - Software vs Direct mapped

		Wideband CDMA			FDMA
		Matched Filter	Trained MMSE	Blind MMSE	Multiple Antenna
Software Programmable (Optimized for DSP)	Parallel Processors	5	11	23	87
	Power (mW)	70	150	300	1150
	Area (mm^2)	115	250	530	2000
Direct Mapped	Power (mW)	.4	1.6	3.1	8
	Area (mm^2)	.6	2	3	10

- ***Software solutions > 100 times less efficient*** (even ignoring overhead of parallel processing)
  - » .5-5 MIPS/mW software DSP (best case) processor
  - » 100-1000 MOPS/mW dedicated

The Potential Computation Efficiency

- In .18 micron – 12x12 multiplier (1 Volt)

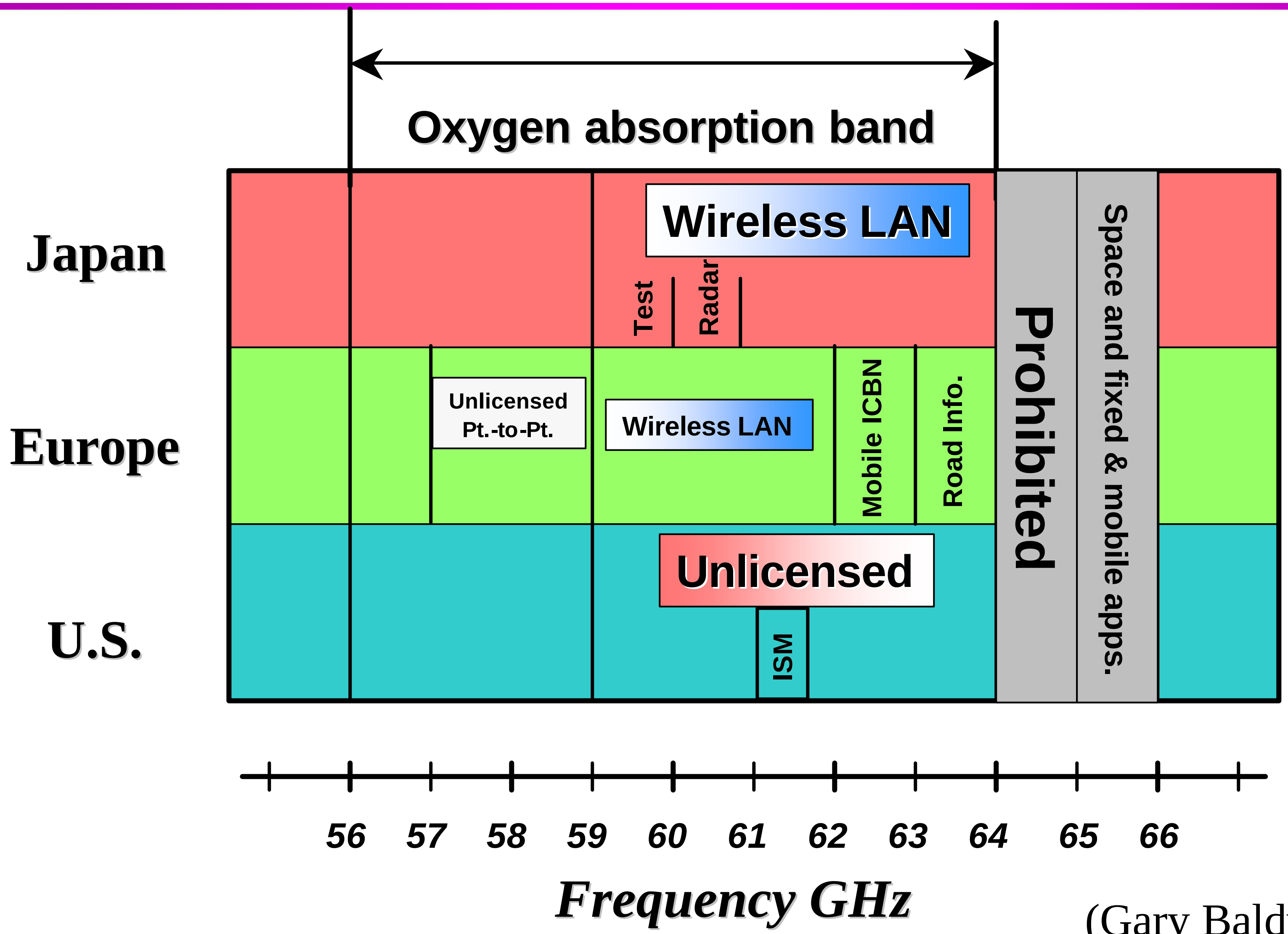
  Area = .03 mm^2

  Energy = 4 μW/MHz (250 Mmult/mW)

  Adder, shifters, registers approx 10 times smaller and more efficient
- Take a chip that has a mix of 400 multipliers and 3600 other elements (adders, shifters, etc…) running at 25 MHz

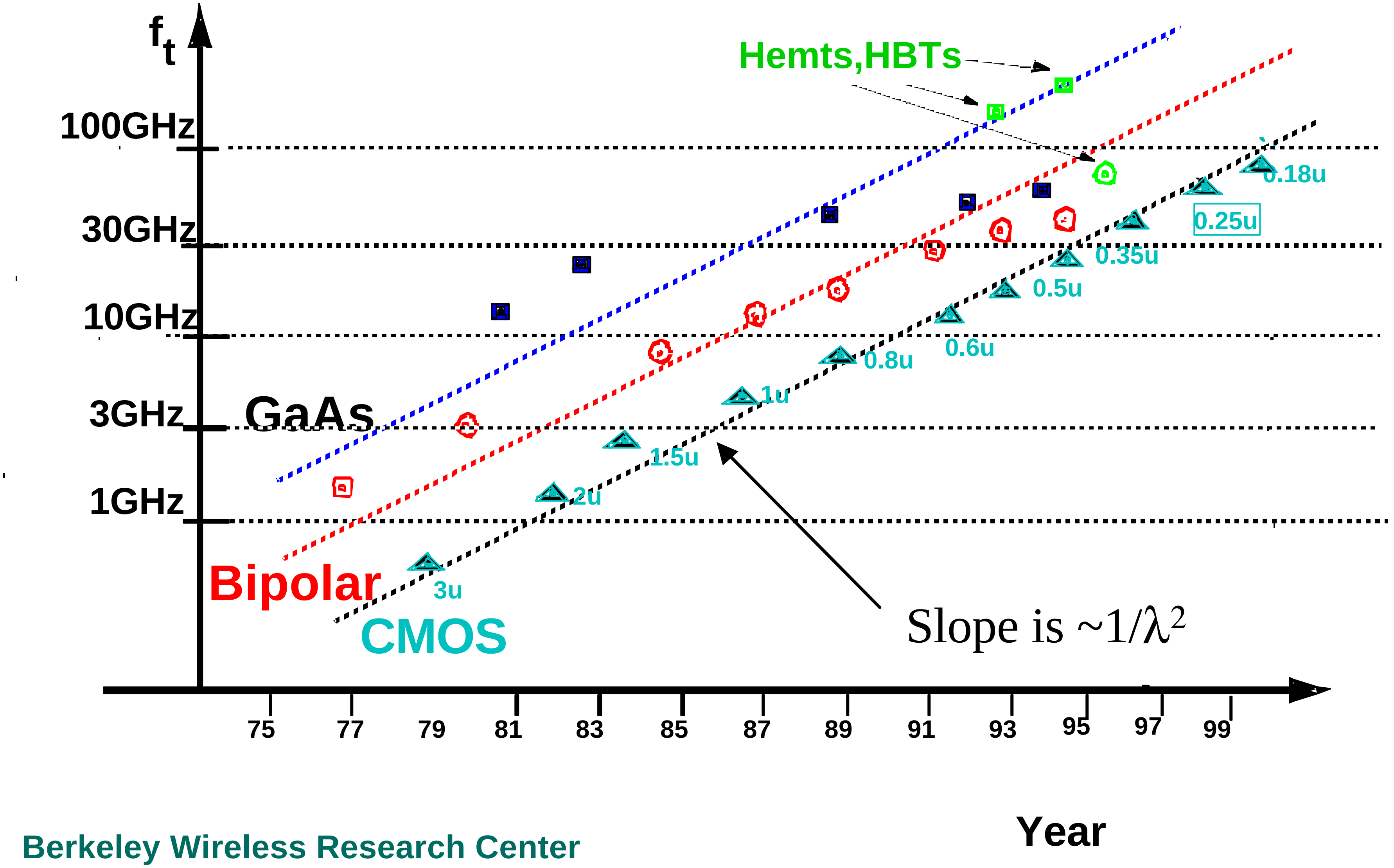
Yields ….100 GOP on $25mm^2$ and 80 milliWatts

Interesting Design Domain - Communications at 60 GHz using CMOS - ***5 GHz** is available*

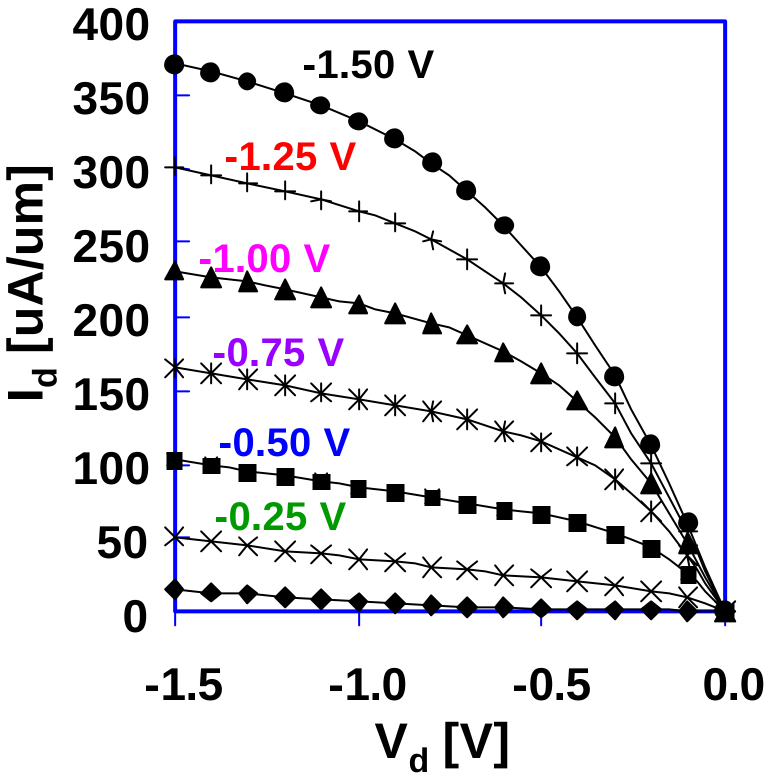


(Gary Baldwin)

Can CMOS do it?



But .018 micron devices exist now!



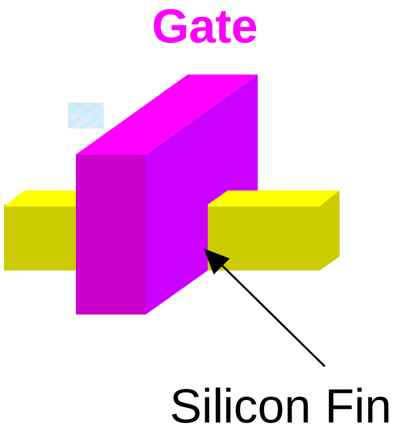
- **FinFet structure**
- **Designed for manufacturability**

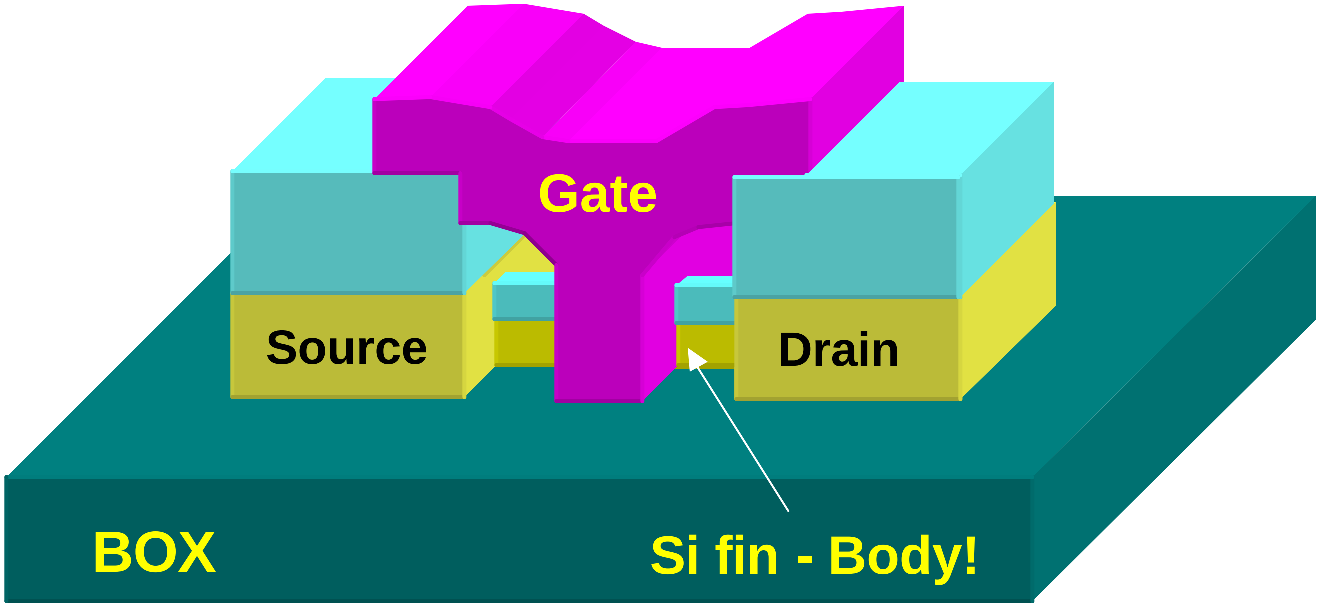
(from Chenming Hu)

FinFET

* Body is a thin silicon Fin *

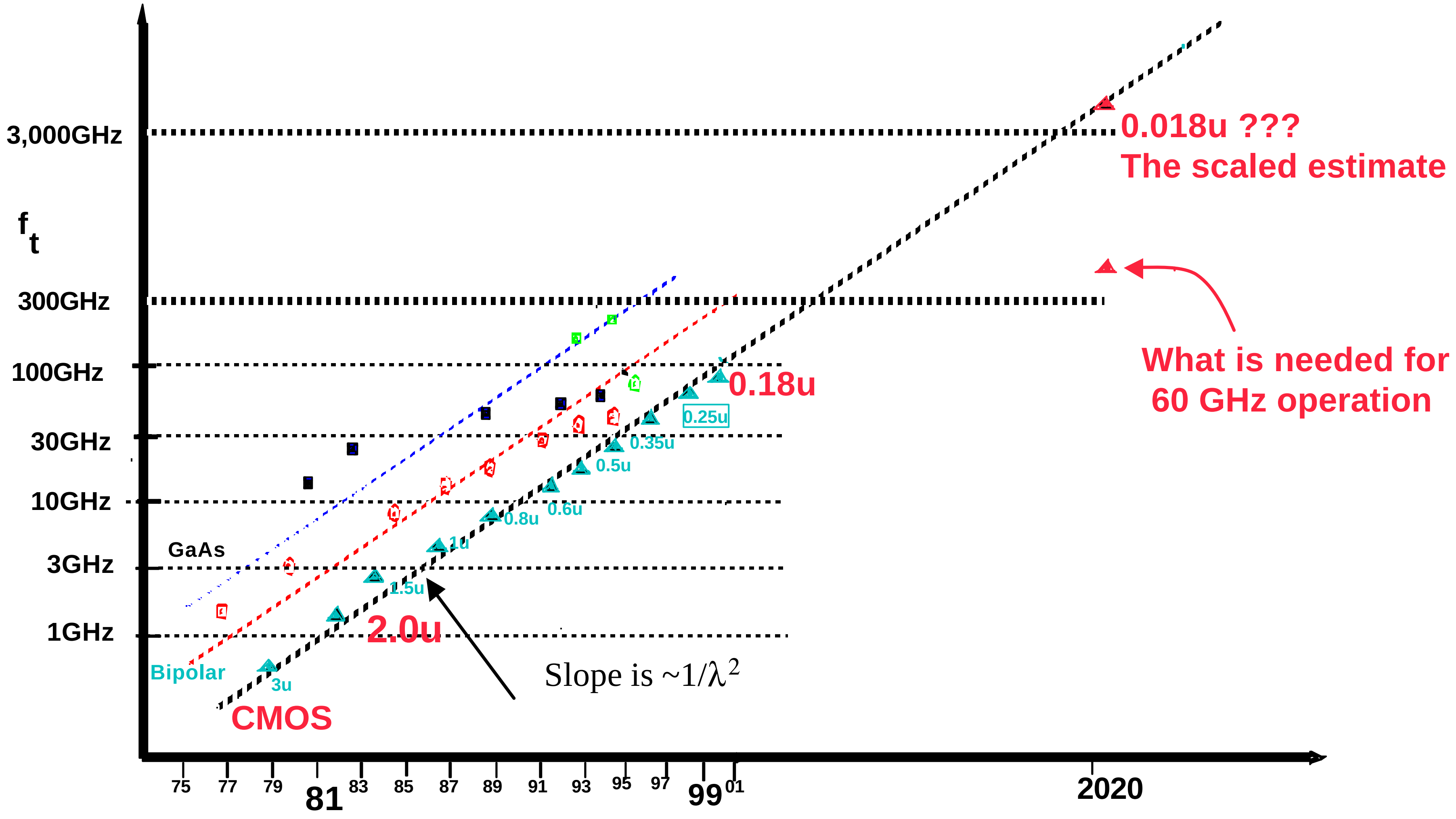
Double-gate structure + raised source/drain





X. Huang, et al, 1999 IEDM, p.67~70

CMOS at 60 GHz



0.018u ???
The scaled estimate

What is needed for
60 GHz operation

Slope is ~$1/\lambda^2$

Achievable Research Goals

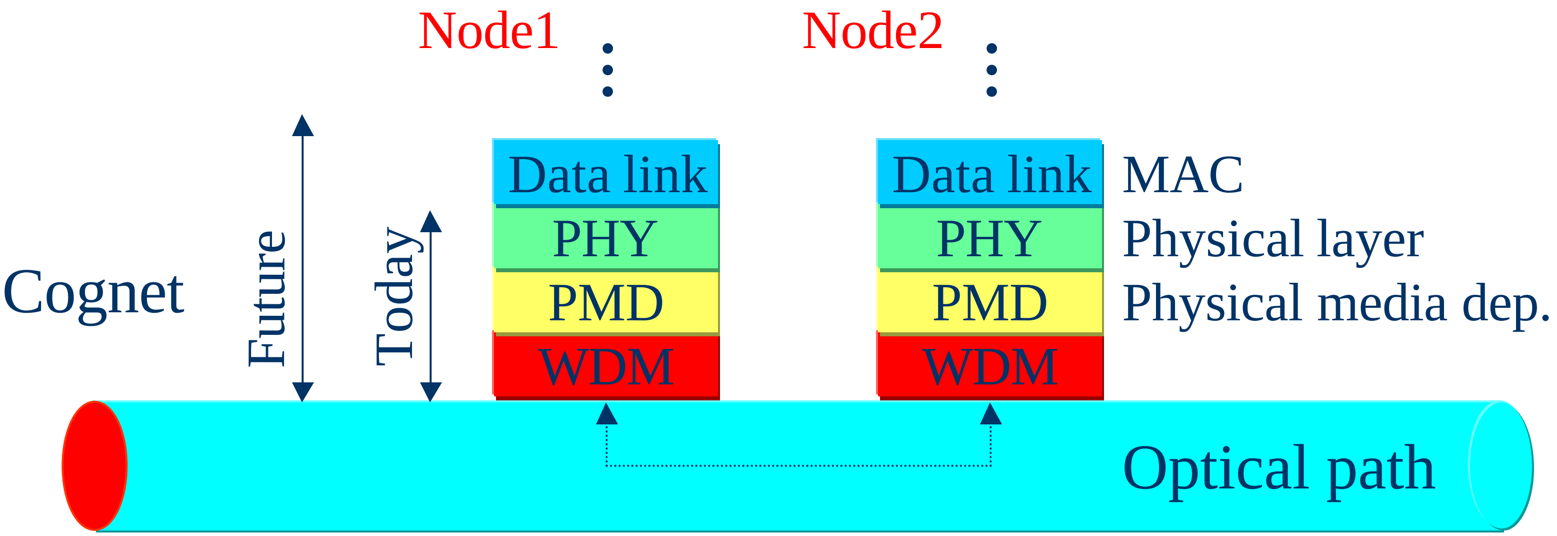
- System-on-a-chip *Design in a Day* from a high level description
  - Fully automated physical design
  - Optimization and estimation of the architectures at the system level
  - Mixed signal design optimization and automatic layout
- Demonstrate computational efficiencies of 1 Teraop/Watt
- Use 60 GHz CMOS communication systems as a driver design domain

Challenges in Design of “Comm-System-on-a-Chip”

Mehdi Kazemi-Nia
Cognet Microsystems
mkazeminia@cognetmicro.com
Tel: 310-231-8242

May, 5th, 2000

Optical Data Networks



cognet microsystems

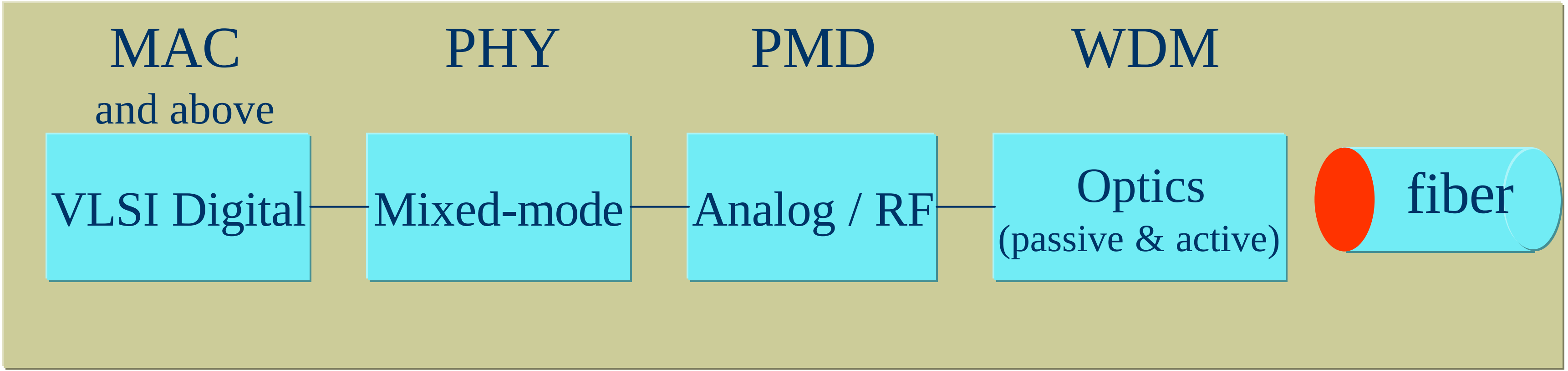
Cognet's Vision

- Provider of low-cost fiber optic solutions for
  - Metro, Local and Access Networks
- Fiber-optic ASIC technology
- Low-cost fully integrated WDM transceiver technology
  - ASICs
  - Optical Mux/Demux

cognet
microsystems

Future SOC Comm Systems

- Heterogeneous integration of optical components with:
  - Analog Radio Frequency circuits (Preamp, Postamp, Laser Driver)
  - Mixed-mode circuits (CDR, A/D, D/A)
  - Digital circuits (SERDES, coding, switch fabric)



Future system simulator

High Quality Inductors on Silicon

- **Why Inductors**
  - Enhance bandwidth (by shunt peaking)
  - Reduce timing jitter (Ex: OC-48 τ_j = 4ps, OC-192 τ_j =1ps …)
- **Challenges**
  - Electromagnetic effects
  - Conductive substrates
  - 3D structure
  - Characterizing noise and crosstalk
    - Noise from digital circuits to low-level analog signals
    - Electromagnetic interference (EMI) generated by HF circuits

cognet microsystems

Challenges in Deep Sub-Micron

- Modeling complexities
- Interconnects
- Design abstraction & Hierarchy
- High-level specification
- More reuse
- Verification

cognet
microsystems

Modeling Complexities

- **Noise side effects on digital design**
    - Noise problem or manufacturing defect?!
    - Isolating timing or functional failures due to noise
    - Noise analysis (by EDA tools) is required to verify the noise level
- High frequency circuit models (including substrate noise)
- Degradation in electrical performance of circuits over time

cognet
microsystems

Modeling Complexities (cont')

- Modeling of interconnect parasitics
    - Significance of wire resistance & rapid increase of coupling capacitance
- Interconnect inductance (accurate 3D model)
    - Global interconnects as lossy transmission lines
- Adequate interconnects models at each level of the design
    - Efficient simulation of full-chip interconnect delay (Trade-off between 2D and 3D)
- For complete systems, including optical & other components
    - Develop CAD methods such as modeling of 3D layout

Interconnect-Limited Designs

- Circuit performance: determined by interconnects instead of devices
- In DSM, interconnect delay will far exceed the device delay!
- Future integrated circuits will be limited by interconnect, not transistors
- Make early consideration of interconnect performance limitation

cognet microsystems

Interconnect-Centric Design Methodology

- Traditional chip design
  - Concentrates on logic functions & ignores interconnects until final step!
  - Signal integrity is a major problem
- Interconnect-driven design
  - Optimized throughout all levels of the process
    - Planning & estimation (allow designers to explore alternatives)
    - Synthesis (topologies, layer assignment, wire widths and spacing, etc)
    - Simulation & Verification (formal verification for performance and reliability)

Abstraction, Hierarchy, Specification

- **Current flow**: behavior, RTL, logic, physical design
  - Decomposing a large system into smaller subsystems

- **Existing abstraction:** incapable of modeling complexity of interconnects

- New challenges to design abstraction and specification
  - Abstractions for function, timing, noise, power
    - Should handle performance, power, etc as well as functionality
  - Designers need high-level specification tools

cognet
microsystems

More Reuse

- Multiple use out of large blocks
  - Standardization of block specifications
  - Include interface timing, power, area
- Using predefined cores
  - Intellectual property (IP) of many varieties need to be integrated
  - Hard core, soft core, firm core
- Methodologies for IP retargeting
  - **Reverse synthesis** (for retargeting of existing modules to new technologies)

Verification

- Must include not only logical function, but noise, timing, etc
  - To make the tools more efficient and to give designers more detailed debugging info
  - Methods and tools combining formal and simulation techniques will be required

- Traditional post layout verification:
  - DRC, ERC (LVS), timing simulation with RC parasitics (back-annotated from layout)

- DSM chips need checking beyond physical design rules and timing delays
  - Signal integrity
  - Power dissipation
  - Reliability (due to potential electro-migration problems)
  - Identifying hot spots in chips
  - EDA tools need to operate in an incremental mode

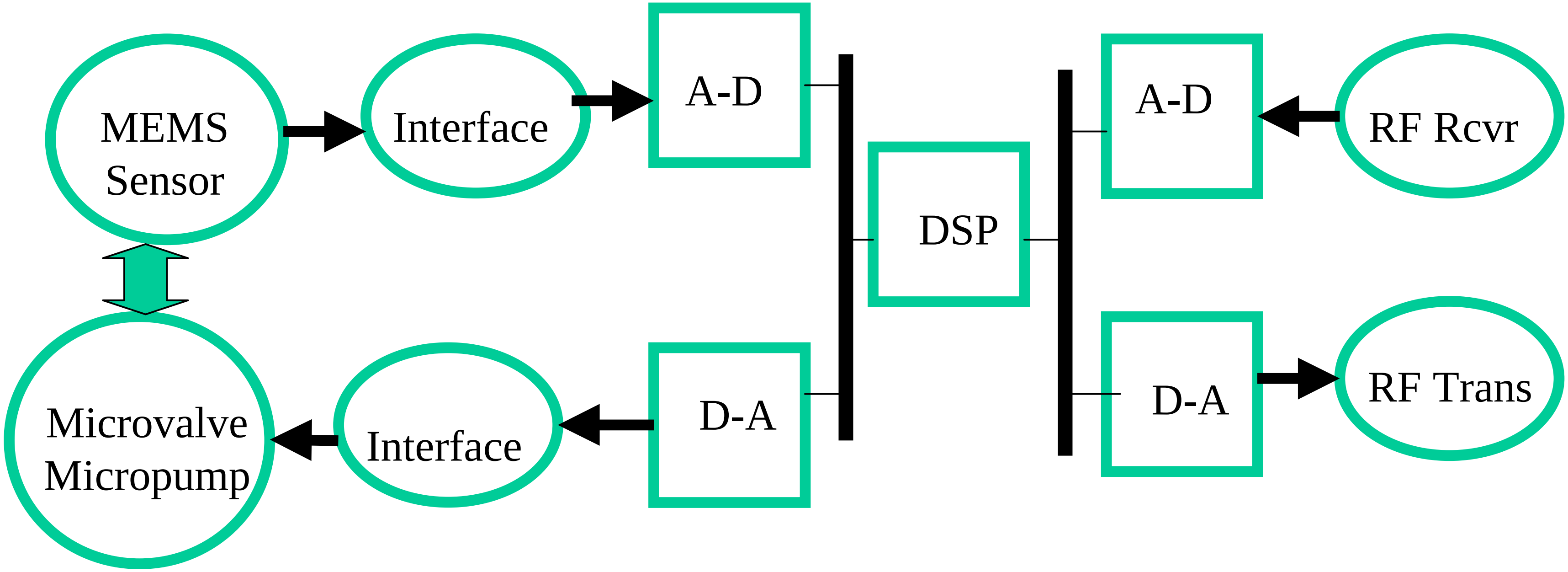
cognet microsystems

Final Challenge

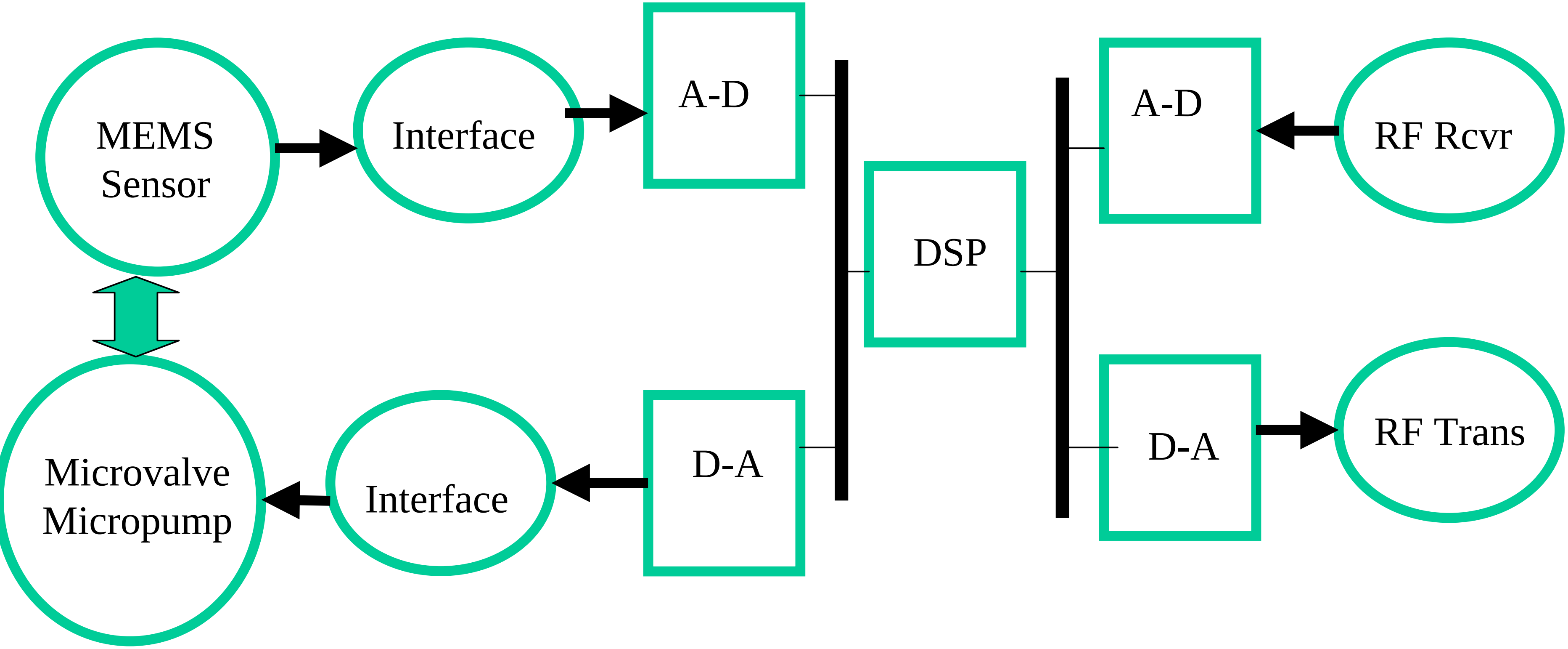
- Packaging
- Testing
- Requires higher level of functional test at the package level

New Technology in Single-Chip Systems- What CAD is needed?

B. Buchmann, J. Kanapka, X. Wang, and J. White, MIT
J. Tausch, SMU, W. Ye, GIT, N. Aluru, UIUC
K. Kundert, K. Nabors, J. Phillips, R. Telichevesky, Cadence
Y. Massoud, Synopsys, M. Kamon, T. Korsmeyer, Microcosm



The Single Chip System - An Example

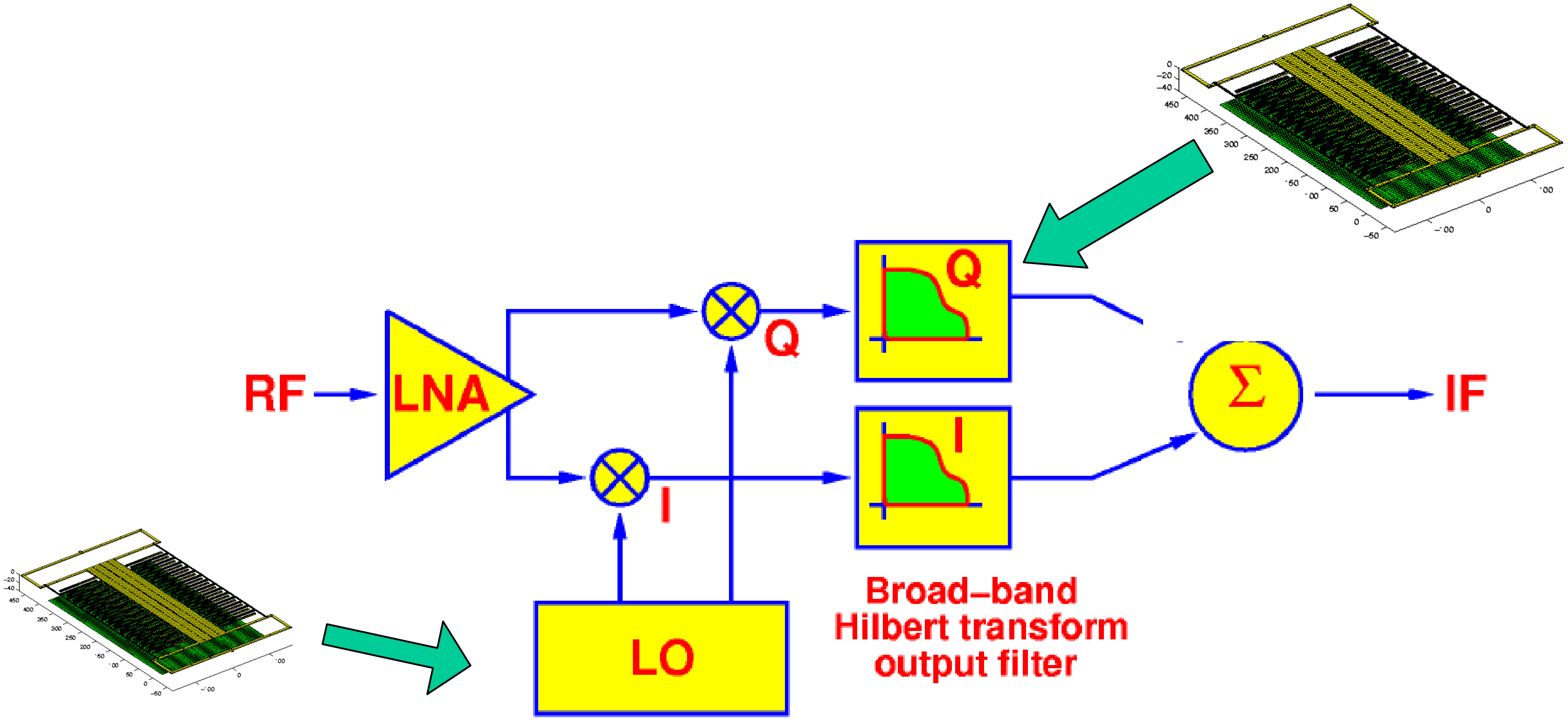


One Chip Chemical Agent Detector

CAD for Diverse Technology in SOC's?

- **Initial Assessment**
  - What is possible with a combination of technology?
  - Will a new technology improve SYSTEM peformance?
  - Requires a rough "optimization" step!
- **System Performance optimization**
  - Assess intra and inter technology trade-offs .
  - What is the impact of fabrication decisions?
  - Automate Analysis and Synthesis/Optimization
- **Manufacturability/Yield optimization**
  - Optimize design considering variations!

An RF-MEMS Example



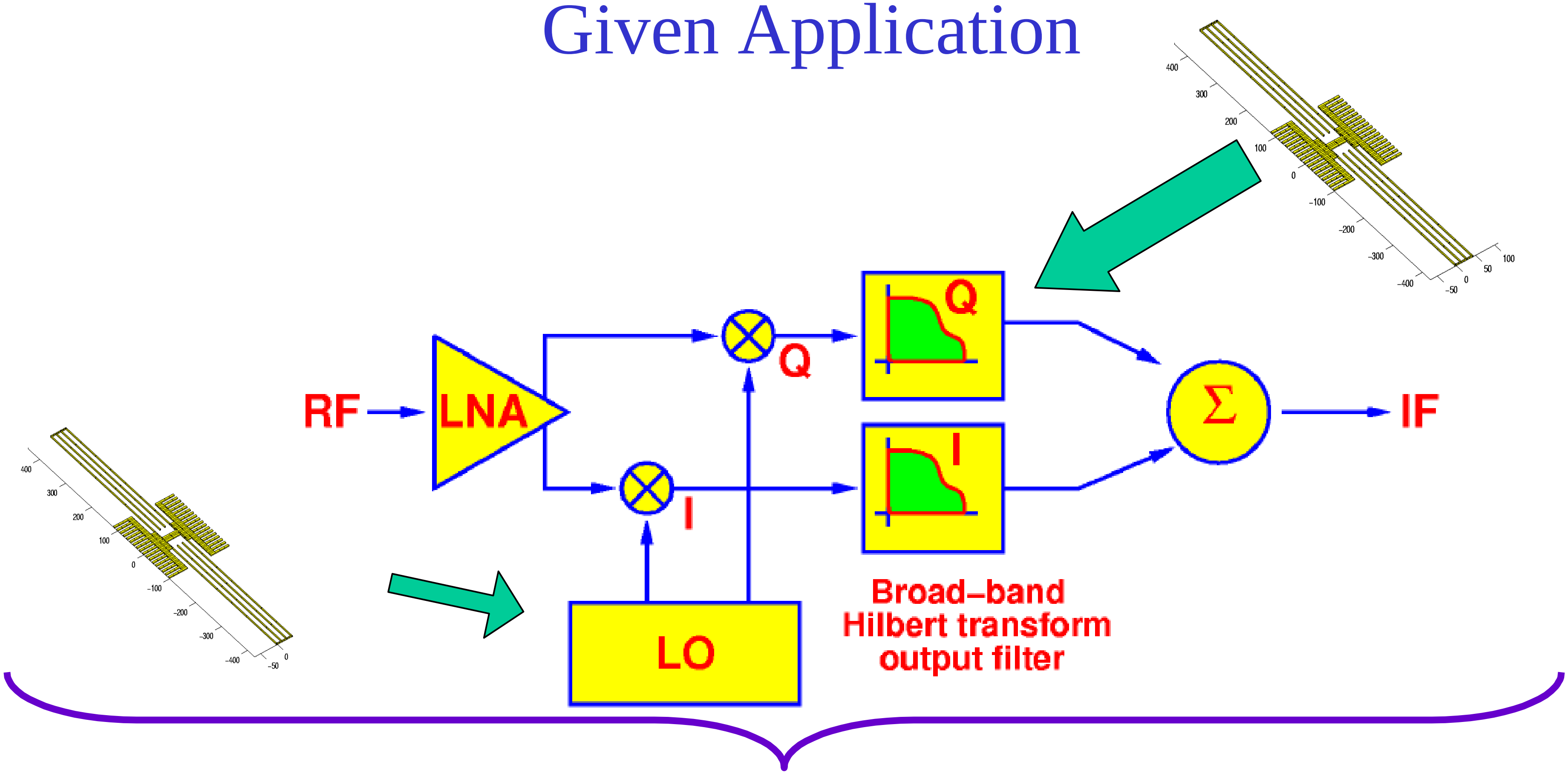
Use Micromachined Filters in an RF Receiver:

- What is system performance (noise, distortion, etc).
- Will poly-substrate separation (changes Q) matter?
- How tight must manufacturing tolerances be?

Need to Assess and Optimize System Performance

- **Hierarchical Simulation**
  - – Encapsulate the physics.
  - – Automatically move between hierarchical levels.
  - – Approach must apply given diverse technology.
- **Hooks for Synthesis/Optimization**
  - – Compute Performance Sensitivities to:
    - Fabrication decisions
    - Layout modifications
    - Architectural Changes.
- **Manufacturability/Yield**
  - – Optimize design considering variations!

Goal: Optimize Micromachined Devices For a Given Application



RF Front end with micromachined resonators for the filter and oscillator

Need to simulate ENTIRE system with dynamically accurate macromodels for the micromachined components

MEMS Model Hierarchy (Nodas: Fedder, Mukherjee)

System models

Device models

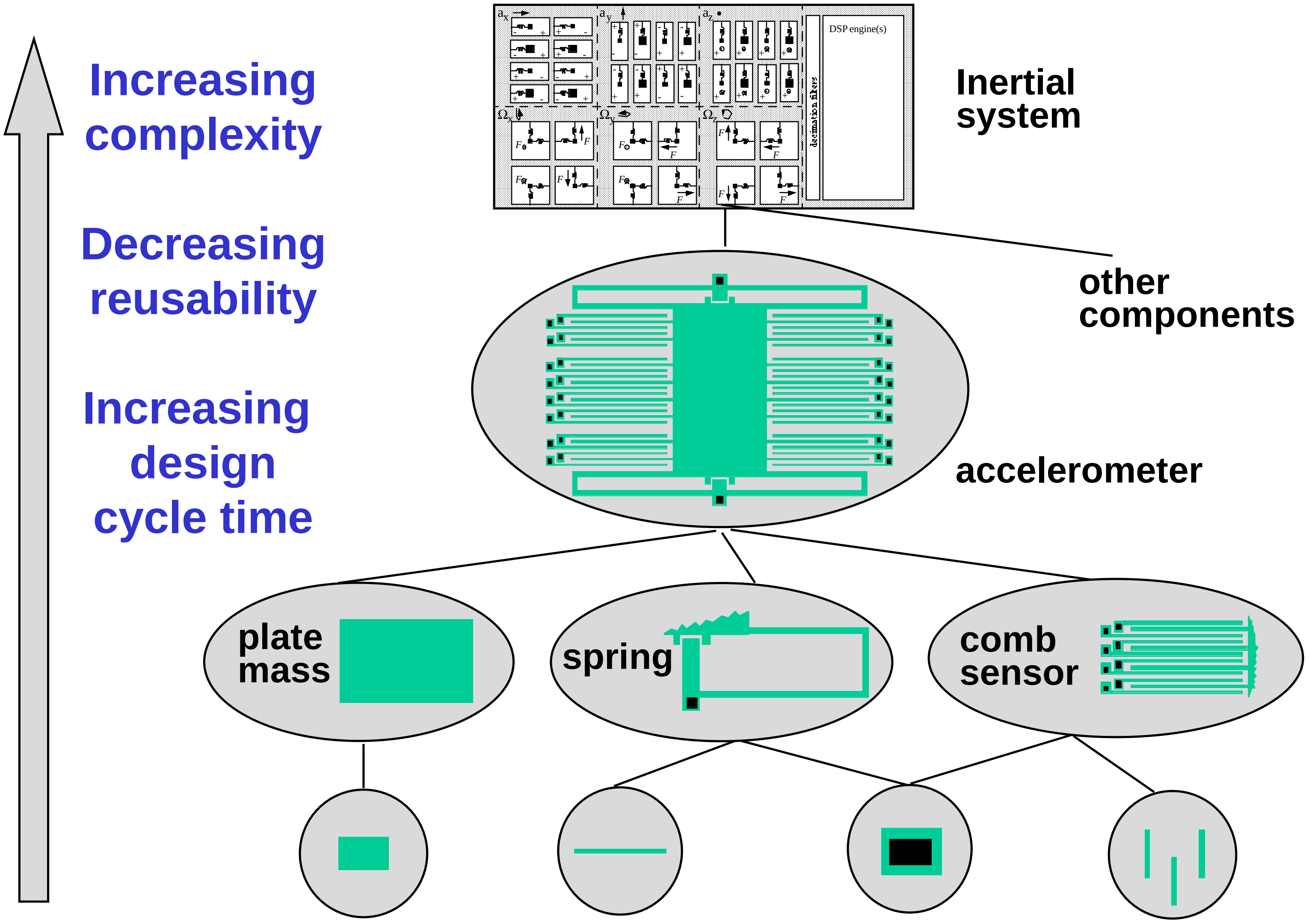
Functional element models

Atomic element models

Increasing complexity

Decreasing reusability

Increasing design cycle time



Inertial system

other components

accelerometer

plate mass

spring

comb sensor

plate

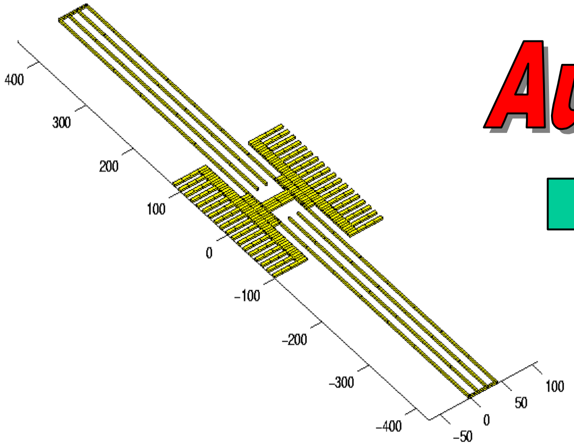
beam

anchor

gap

The Numerical Macromodeling Paradigm

Generate a Reduced-Order Model Directly from 3-D Geometry and Physics



Automatic

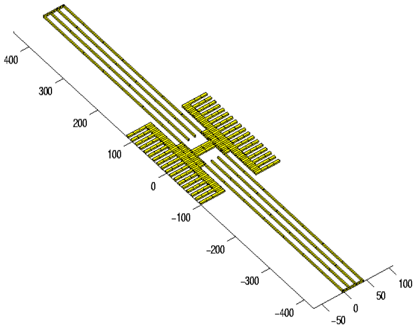
$$\frac{dx_r(t)}{dt} = F(x_r(t)) + b_r u(t)$$

$$y(t) = c_r^T x_r(t)$$

Complicated Geometry,
Coupled Electrostatics,
Fluids, Elastics

Low order state-space
model which captures
input (u)/output(y)
behavior

What’s Needed For Numerical Macromodeling



$$\frac{dx_r(t)}{dt} = F(x_r(t)) + b_r u(t)$$

$$y(t) = c_r^T x_r(t)$$

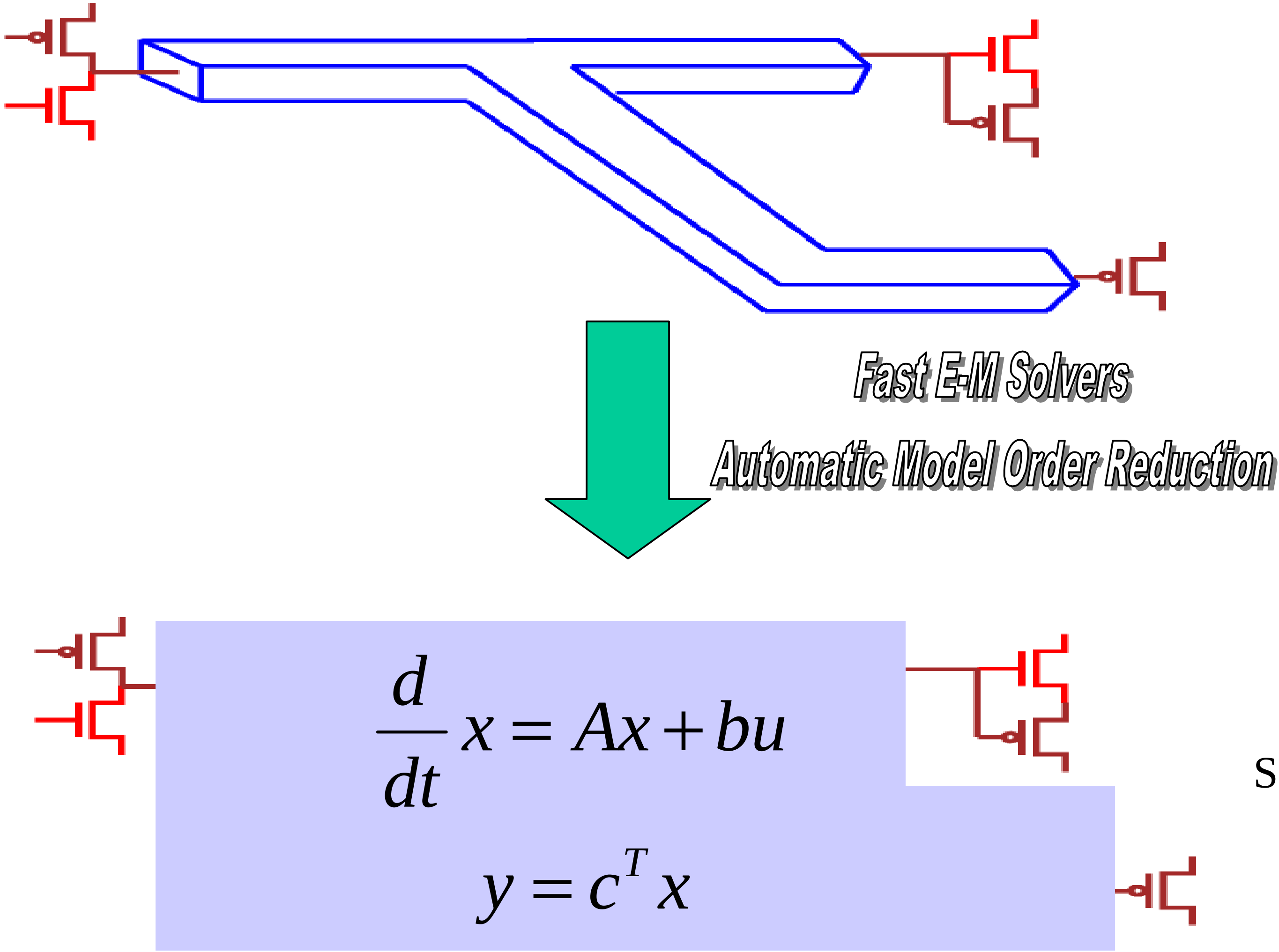
1) Fast Coupled Domain 3-D Solvers

- Fluids, EM Fields, mechanics
- Must handle ENTIRE Devices!
- Lots of recent progress:
  - **Matrix-Free Multilevel Newton, FastCap, FastStokes**

2) Model-Order Reduction

- Start with a Meshed 3-D Structure (>100,000 DOF’s)
- Automatic generation of low-order model (<100 DOF’s)
  - **Linearized approaches, guided approaches**

Where Are We Now? - Linear is “easy”!



Fast E-M Solvers

Automatic Model Order Reduction

$$\frac{d}{dt}x = Ax + bu$$

$$y = c^T x$$

Five years ago

Coupled Circuit
Electromagnetic
Simulation

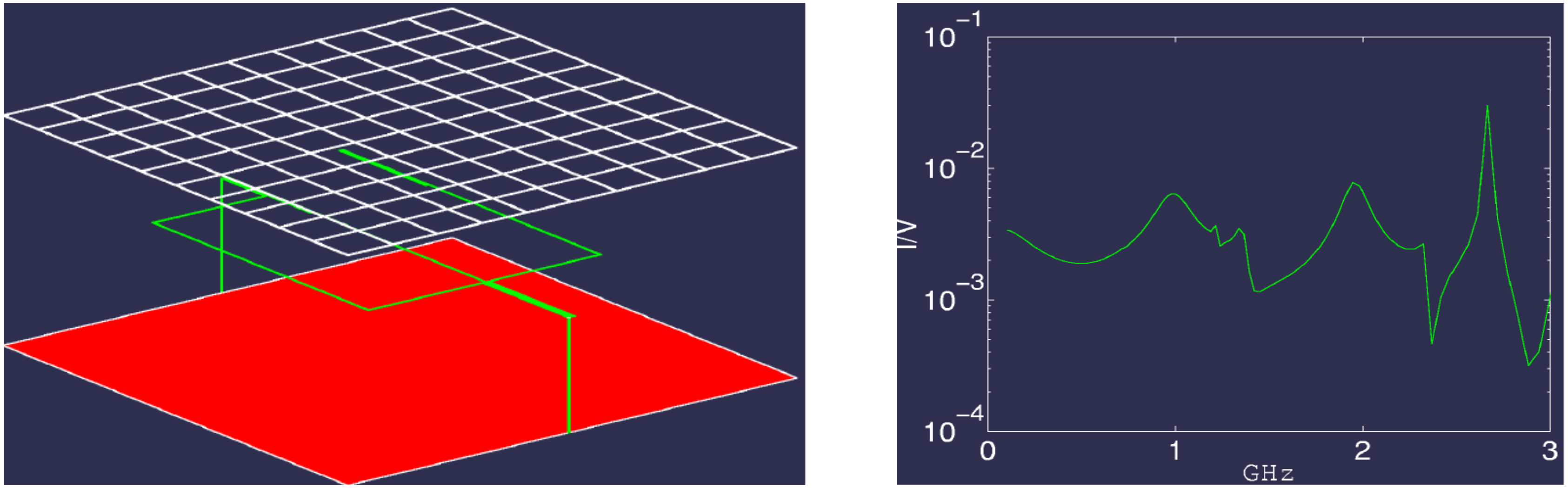
~10 Transistors

Now

Fast Circuit-Level
Simulation Algorithms
and MOR

~1000 Transistors

Fast Wideband Integral Equation Solvers Plus Automatic Reduced-Order Model Generation



Input Impedance for a Transmission line between a solid and a meshed plane

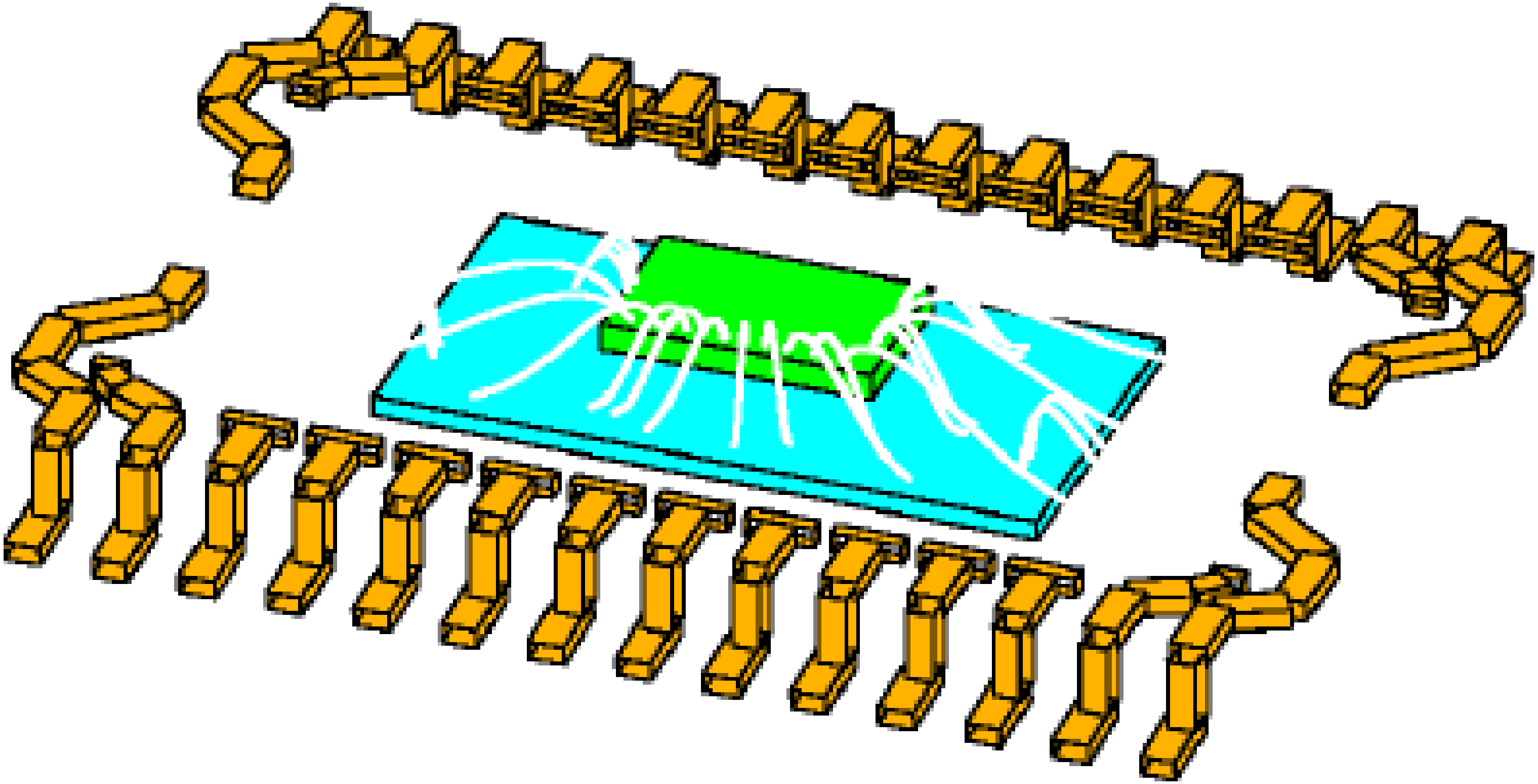
Key Accomplishments:

•First Fast MOM Solver for Full Wave (Precorrected-FFT)

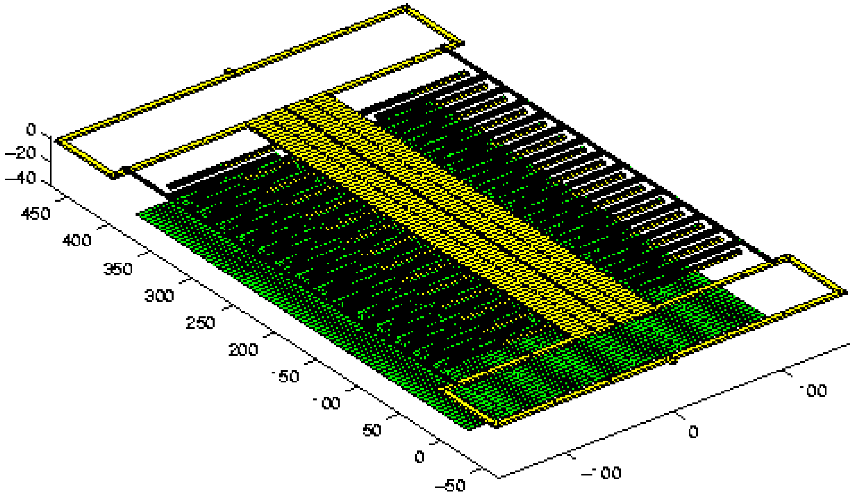
• First Krylov-subspace based Reduction Strategy for MOM

•Orders of Magnitude Faster (Direct-200 Days, Fast-1 day)

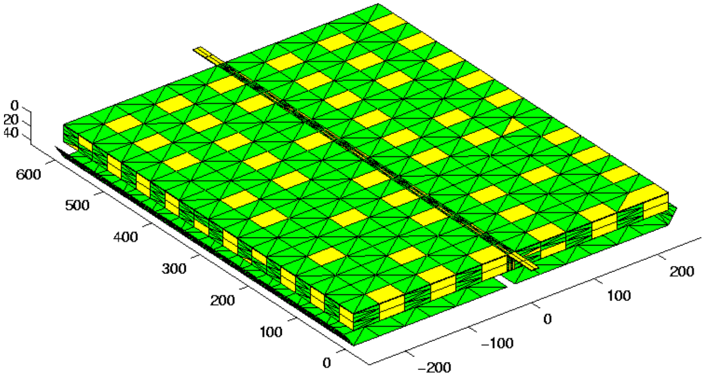
Automatically Generated models of IC Packages



Dynamic Macromodels for Linearized Problems



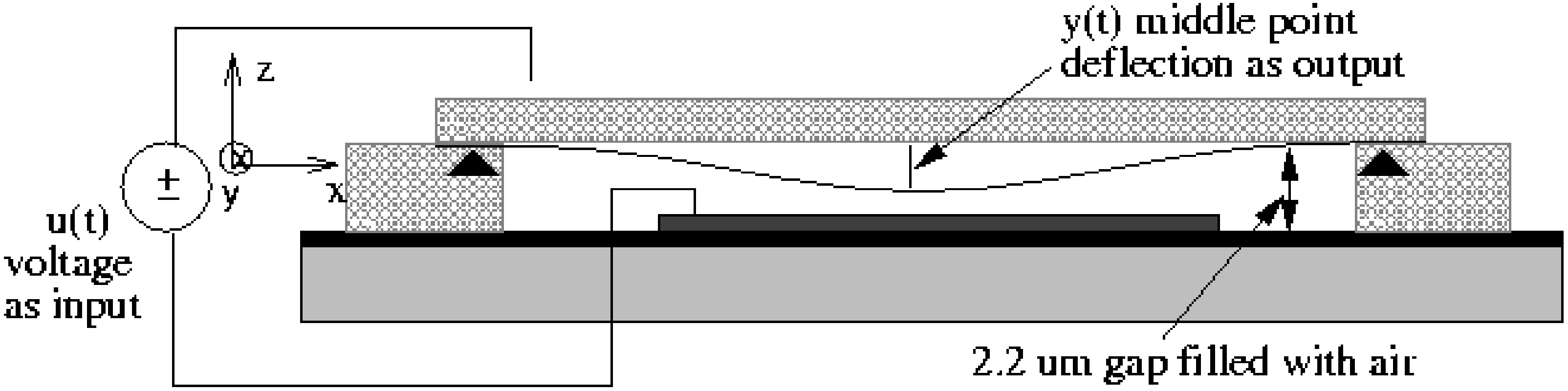
Comb Accelerometer



Scanning Mirror

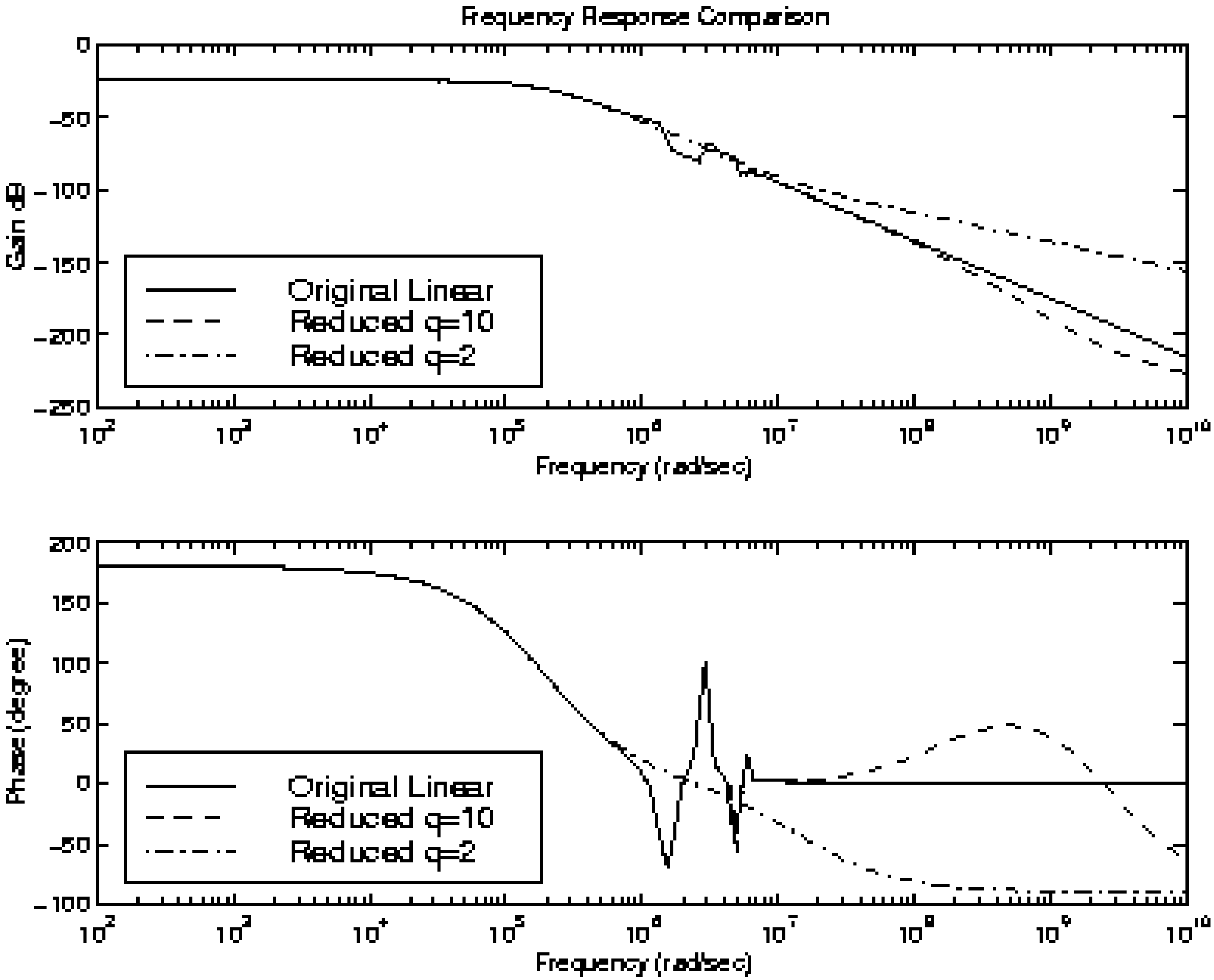
- **Accelerometer and Mirror can operate in Small Signal**
  - Coupled Domain (Fluids, Electrostatics, Mechanics)
  - Need Dynamically Accurate Macromodels automatically extracted from simulation

Deforming Beam Example Problem



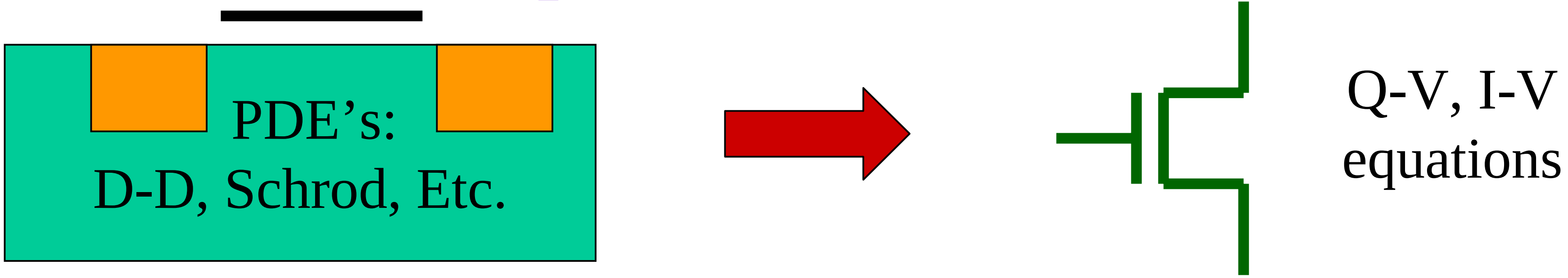
- Coupled Mechanics (Beam), Fluids (squeeze film), and Electrostatics
- Spatial Discretization generates a large ODE System
- Using Position and Velocity yields State-Space Normal Form

Excellent Frequency Domain Match



What if we could do nonlinear model-order reduction?

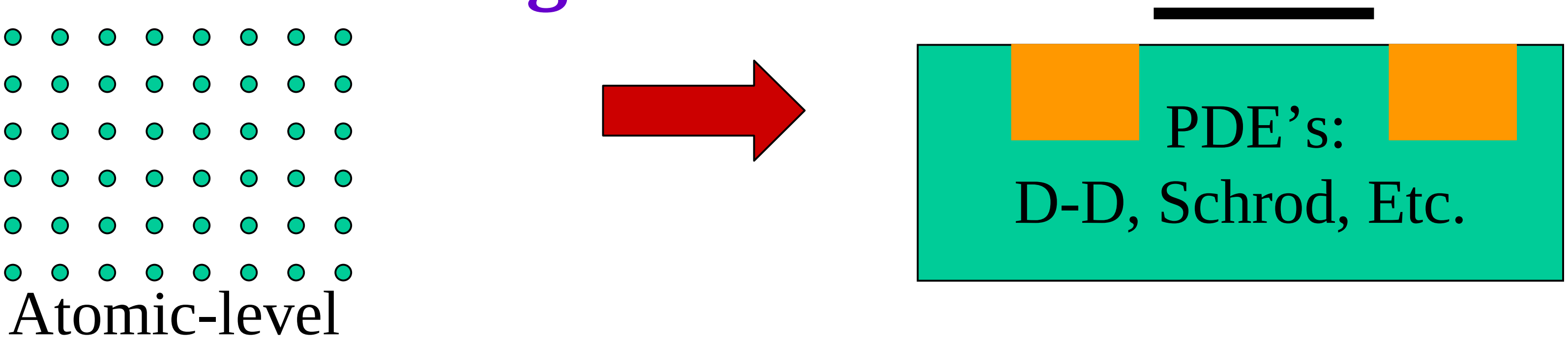
- **Automatic Compact Model Generation**



PDE’s:
D-D, Schrod, Etc.

Q-V, I-V
equations

- **Multiscale modeling?**



Atomic-level

PDE’s:
D-D, Schrod, Etc.

- **New device/technology models**

Valve

$$\frac{dx_r(t)}{dt} = F(x_r(t)) + b_r u(t)$$

$$y(t) = c_r^T x_r(t)$$

State-Space-Based Linear Model Order Reduction

- Spatial discretization generates a *LARGE (>10,000) System of ODES*

$$\frac{d}{dt}x = Ax + bu, \quad y = c^T x$$

Input=u,
output=y,
state=x

- Examine the transfer function of the system using Laplace

$$H(s) = -c^T (I - sA^{-1})^{-1} A^{-1} b \;=\; \sum_{k=0}^{\infty} c^T A^{-(k+1)} b s^k$$

Taylor Series
in s

- Find a small system whose transfer function is "similar".

$$\frac{d}{dt}x_r = A_r x_r + b_r u \quad y_r = c_r^T x_r$$

Small State space

Projection Framework - Linear Case

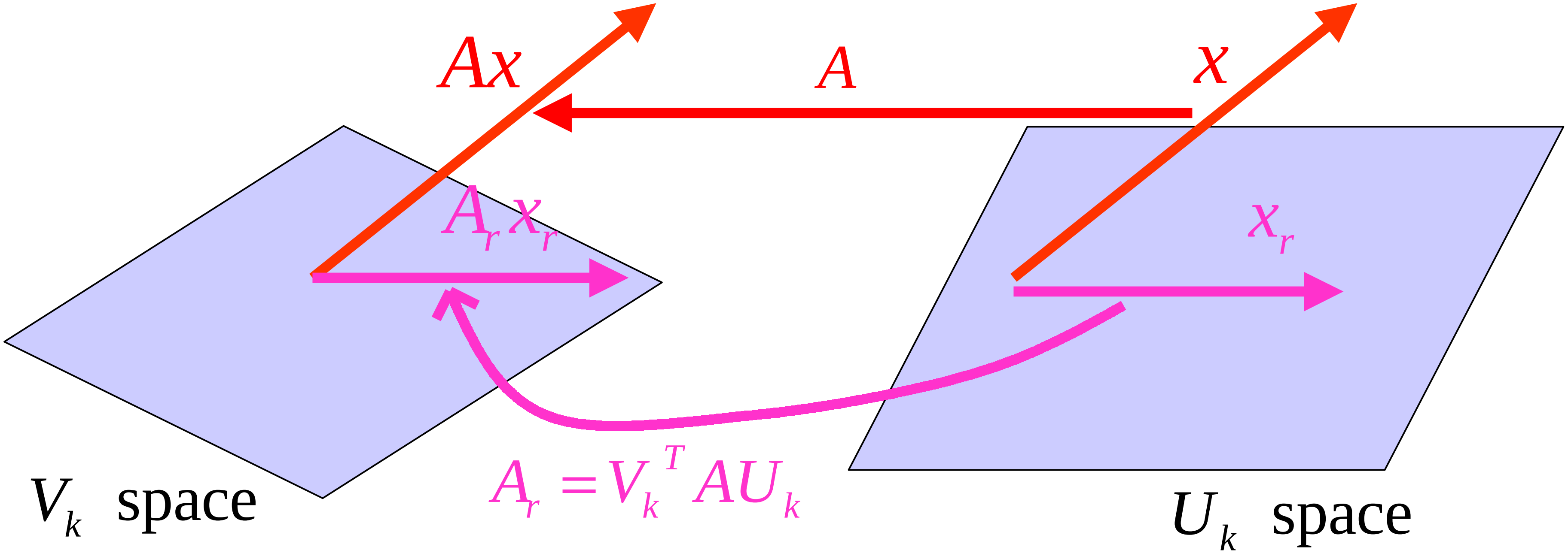
$$\frac{dx}{dt} = Ax + bu,\ \ y = c^T x \Rightarrow \frac{dx_r}{dt} = A_r x_r + b_r u,\ \ y_r = c_r^T x$$

Equation Testing

$$V_k^T Ax = A_r x_r$$

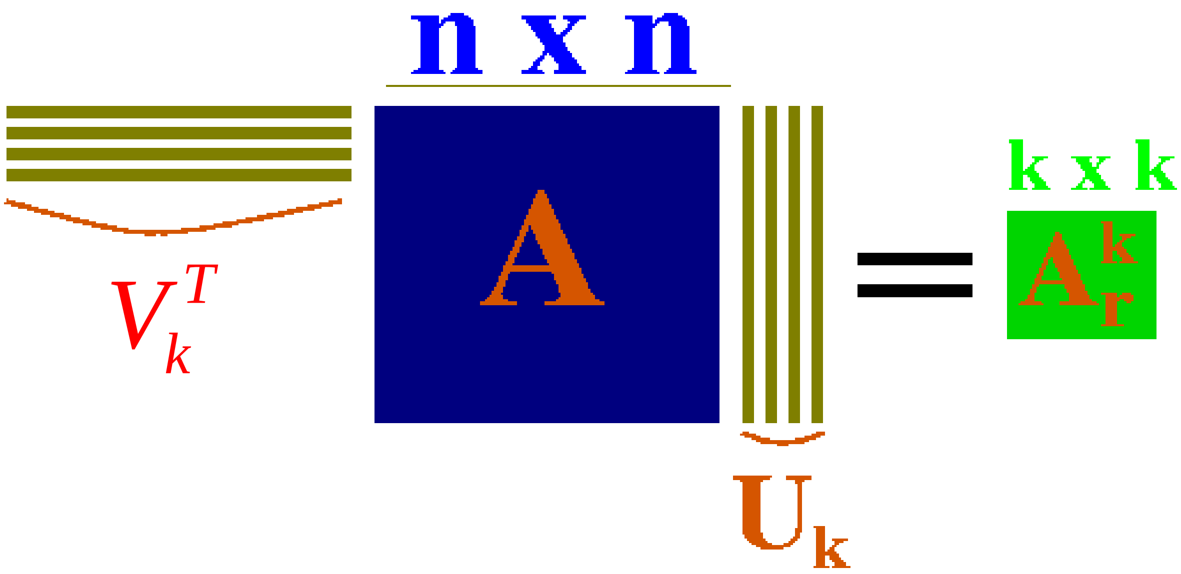
Change of variables

$$x = U_k x_r$$



Galerkin $\rightarrow V_k$ space = U_k space

Projection Yields Explicit Reduced Matrix



- Do NOT need A explicitly, just way to compute Ax

  For each column of U_k

  Multiply by A, then dot with columns of V_k

How to pick U and V? - There are ways.

Nonlinear Model Order Reduction

- Spatial discretization generates a *LARGE (>10,000) System of ODES*

$$\frac{d}{dt}x = F\left(x\right) + bu, \;\; y = c^T x$$

Input=u,
output=y,
state=x

- ~~Examine the transfer function of the system using Laplace~~

  - Find a small system whose input/output is “similar”.

$$\frac{d}{dt}x_r = F_r\left(x_r\right) + b_r u \quad y_r = \left(c_r\right)^T x_r$$

Small State space

Projection Framework - Nonlinear Case

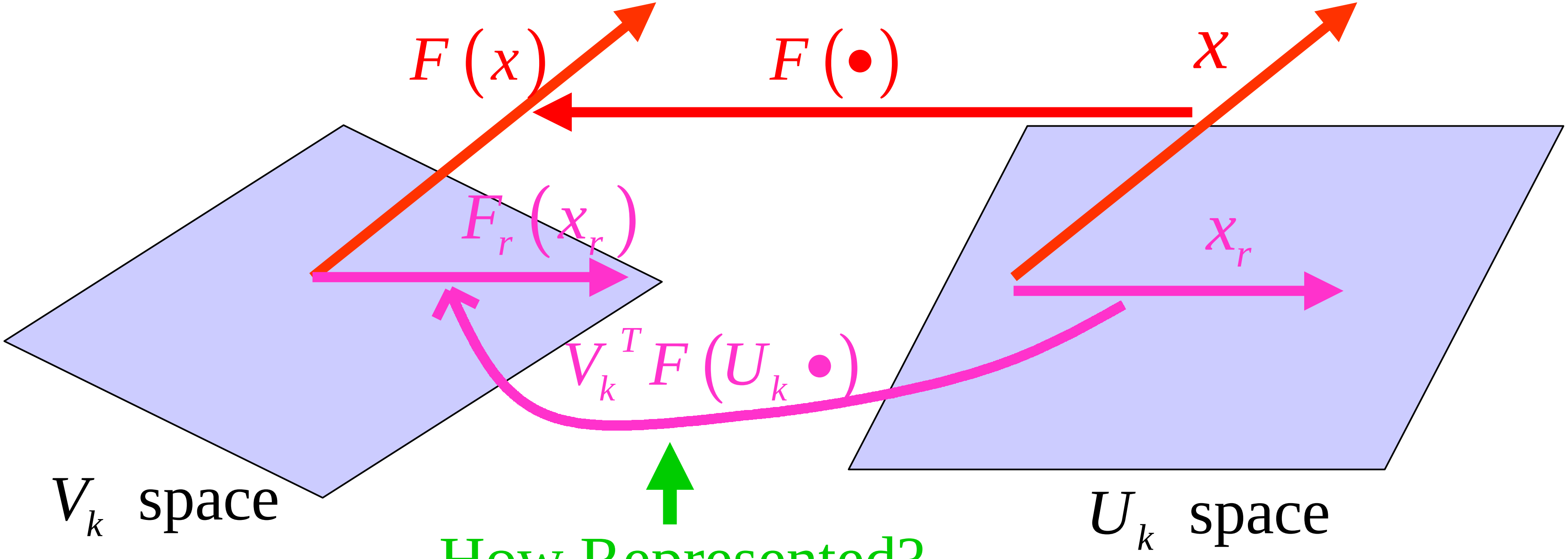
$$\frac{dx}{dt} = F(x) + bu, \;\; y = c^T x \;\Rightarrow\; \frac{dx_r}{dt} = F_r(x_r) + b_r u, \;\; y_r = c_r^T x$$

<u>Equation Testing</u>

$$V_k^T F(x) = F_r(x_r)$$

<u>Change of variables</u>

$$x = U_k x_r$$



$F(x)$

$F(\bullet)$

x

$F_r(x_r)$

x_r

$V_k^T F(U_k \bullet)$

V_k space

U_k space

How Represented?

State-Space-Based Quadratic Model Order Reduction

- Spatial discretization generates a *LARGE (>10,000) System of ODES*

$$\frac{d}{dt}x = F\left(x\right) + bu, \quad y = c^T x$$

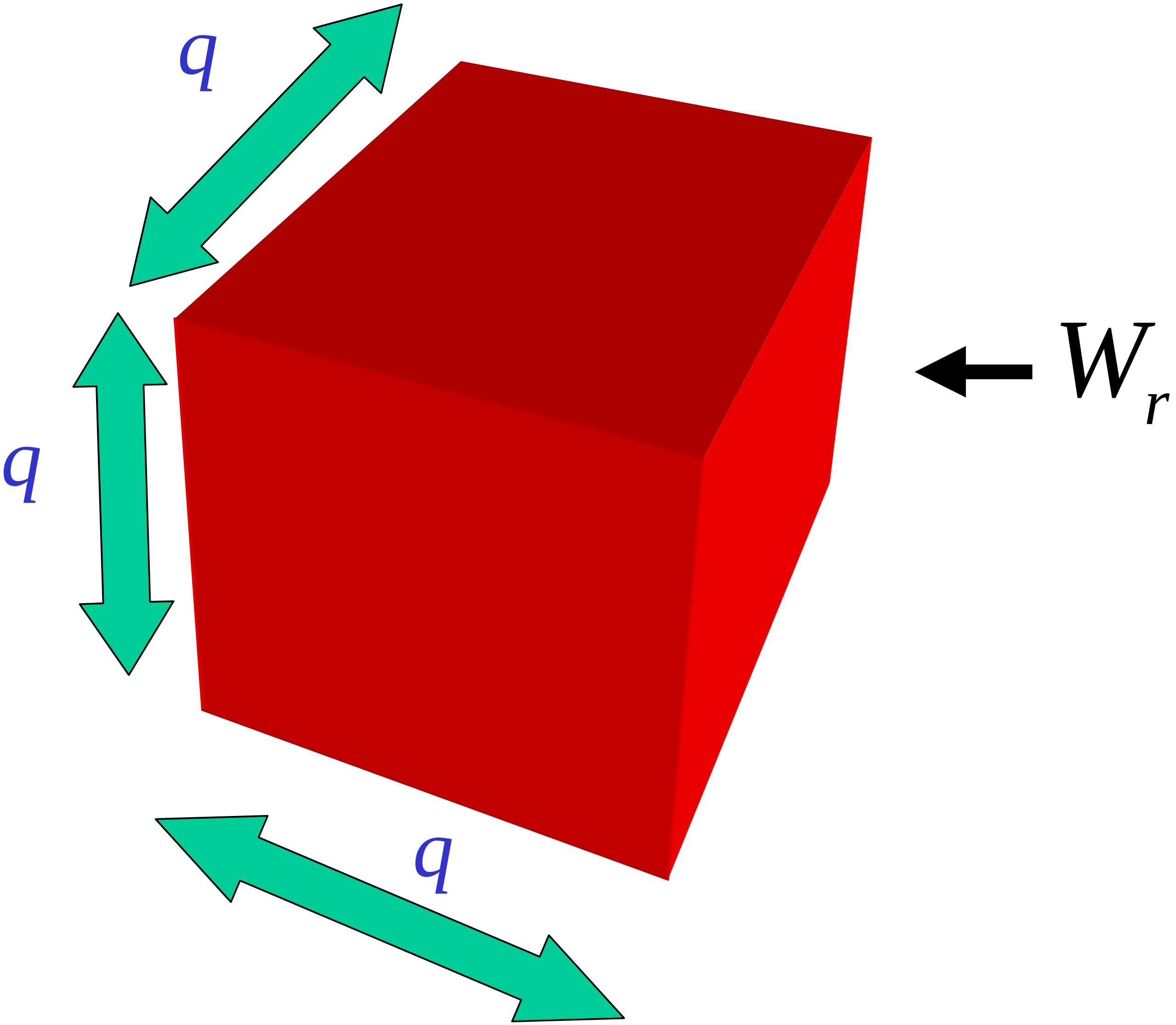
- Taylor Series expand F to second order

$$\frac{d}{dt}x = Jx + x^T W x + bu, \quad y = c^T x$$

- Find a smaller quadratic system.

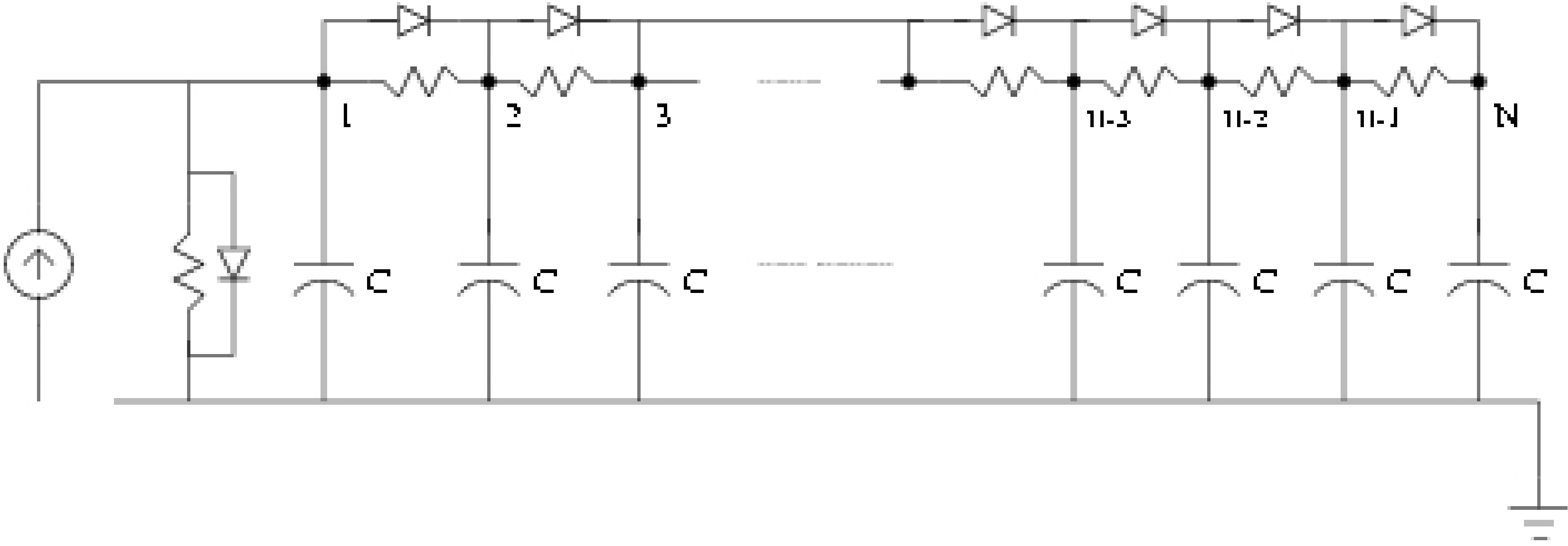
$$\frac{d}{dt}x_r = J_r x_r + x_r^T W_r x_r + b_r u \quad y_r = c_r^T x_r$$

W_r has q^3 entries

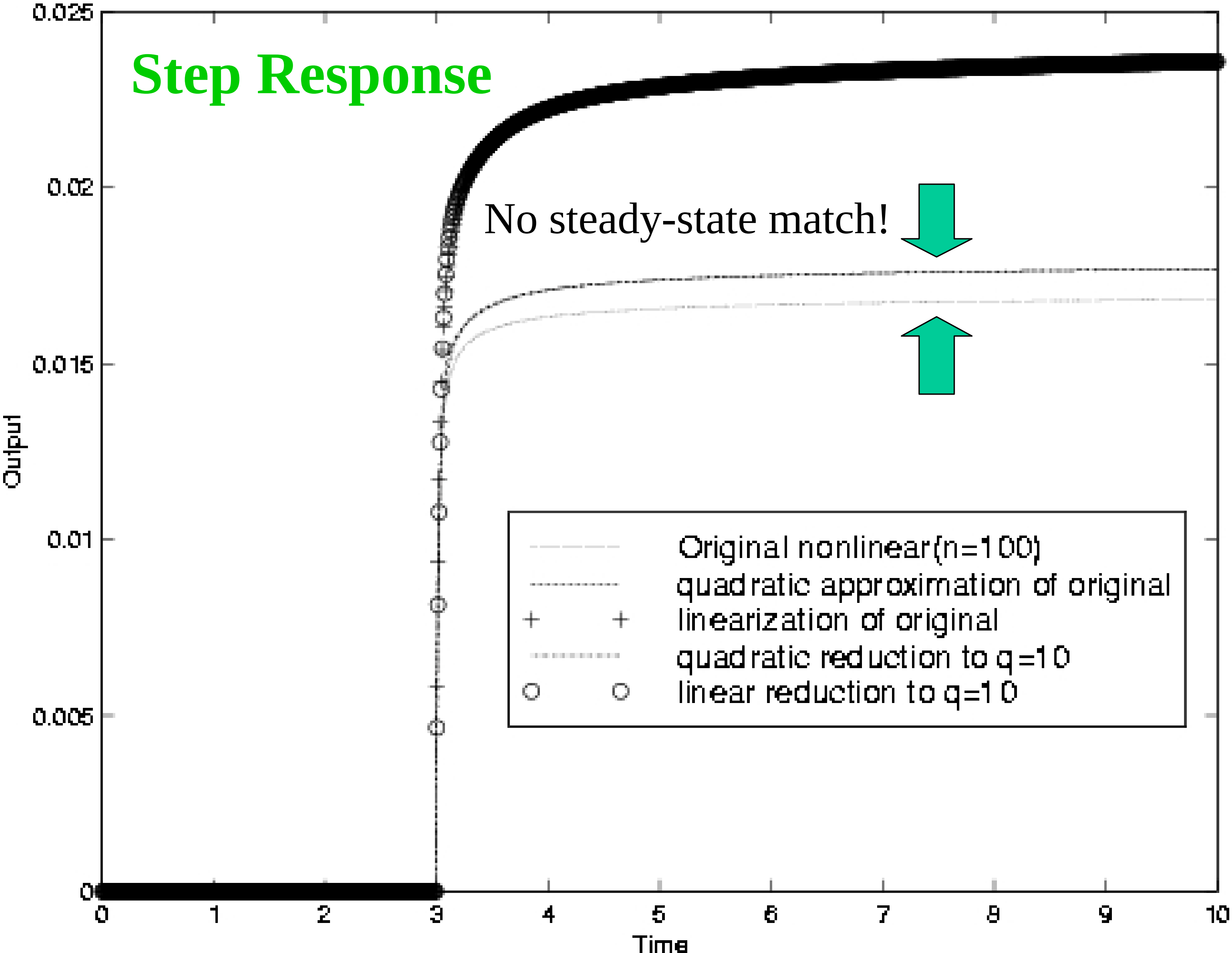


State-Space-Based Nonlinear Model Order Reduction - Projection Using Linearized Arnoldi Vectors

Nonlinear Diode Network Example



Step Response



No steady-state match!

Higher Order Model Order Reduction Grows Exponentially!!!

- Find a smaller higher order system.

$$\frac{d}{dt}x_r = J^0 x_r + J_r^1(x_r \otimes x_r) + J_r^2\left(x_r \otimes x_r \otimes x_r\right) + \ldots + bu$$

- The reduced matrices are DENSE and LARGE.

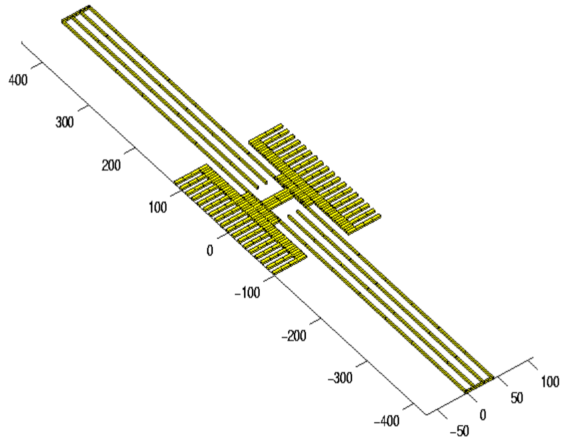
J_r^0 is $q \times q$, J_r^1 is $q \times q^2$, J_r^2 is $q \times q^3$

J_r^3 for a 20*th* order quartic model, 320,000 terms!!!!

- The key problem is automatic sparsification!

For J_r^3, is every term $x_{r_i} x_{r_j} x_{r_k} x_{r_l}$, $i, j, k, l \in \{1, \ldots, q\}$ needed?

What’s Needed For Nonlinear Numerical Model Reduction?



$$\frac{dx_r(t)}{dt} = F(x_r(t)) + b_r u(t)$$

$$y(t) = c_r^T x_r(t)$$

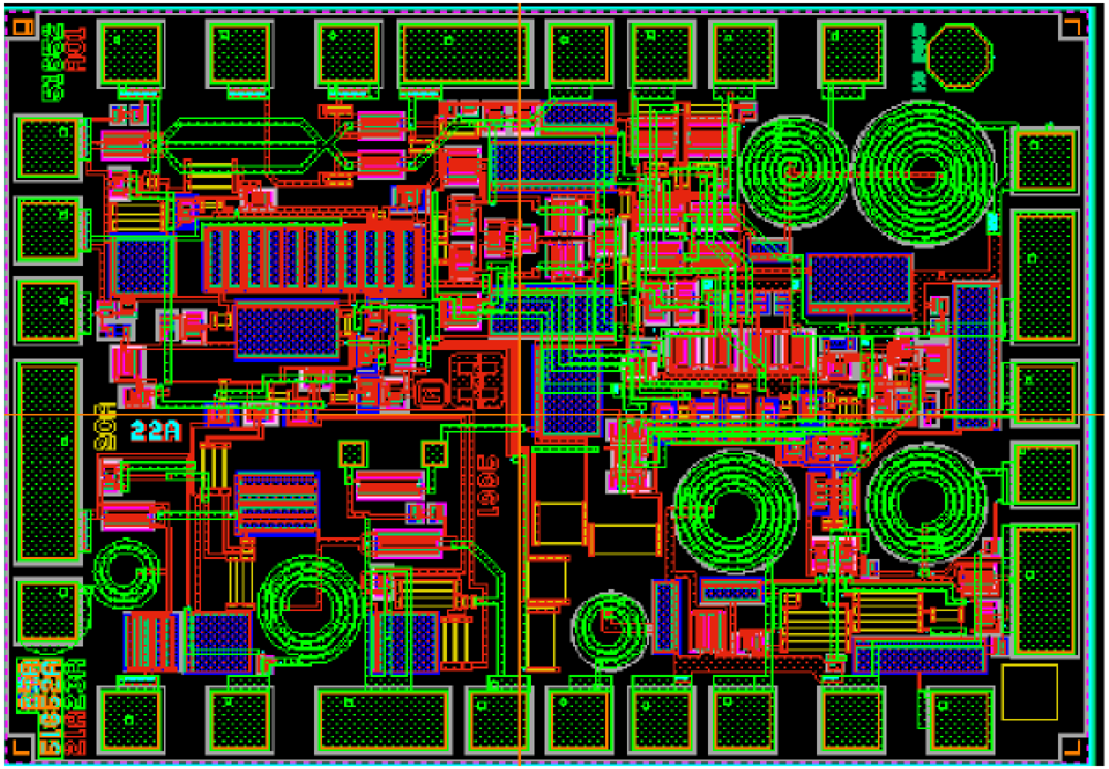
1) Fast Nonlinear Coupled Domain 3-D Solvers

- Most fast solvers for linear problems.
- E.G. - Compressible- or Navier- Stokes

2) Nonlinear Numerical Model-Order Reduction

- Select the projection directions.
- Find sparse representation of reduced F.

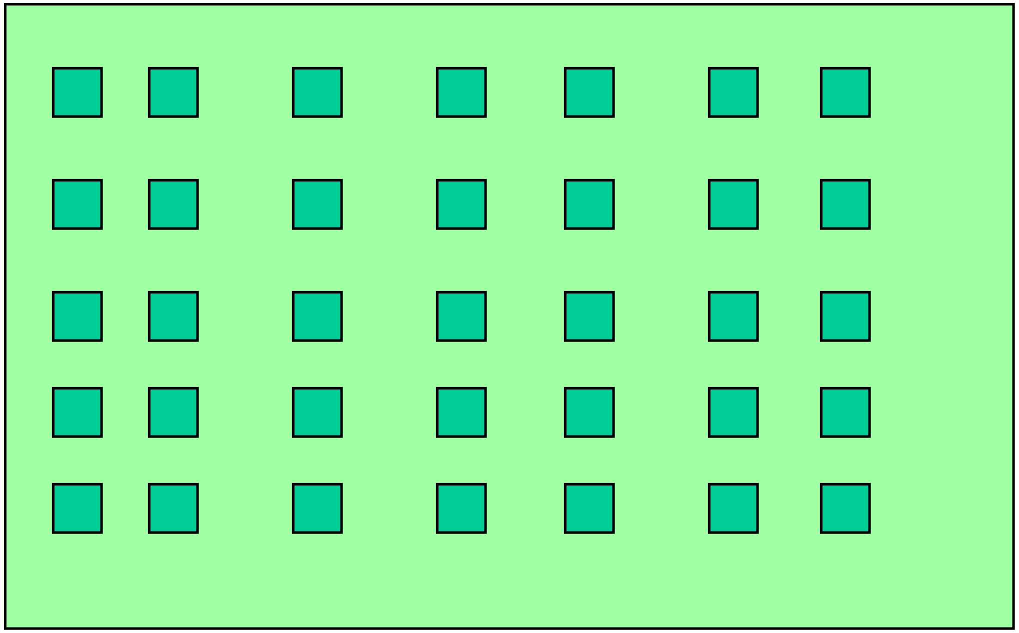
No Good Solutions for Massively Coupled Problems



Chip Layout for
a 900 Mhz RF
Front End

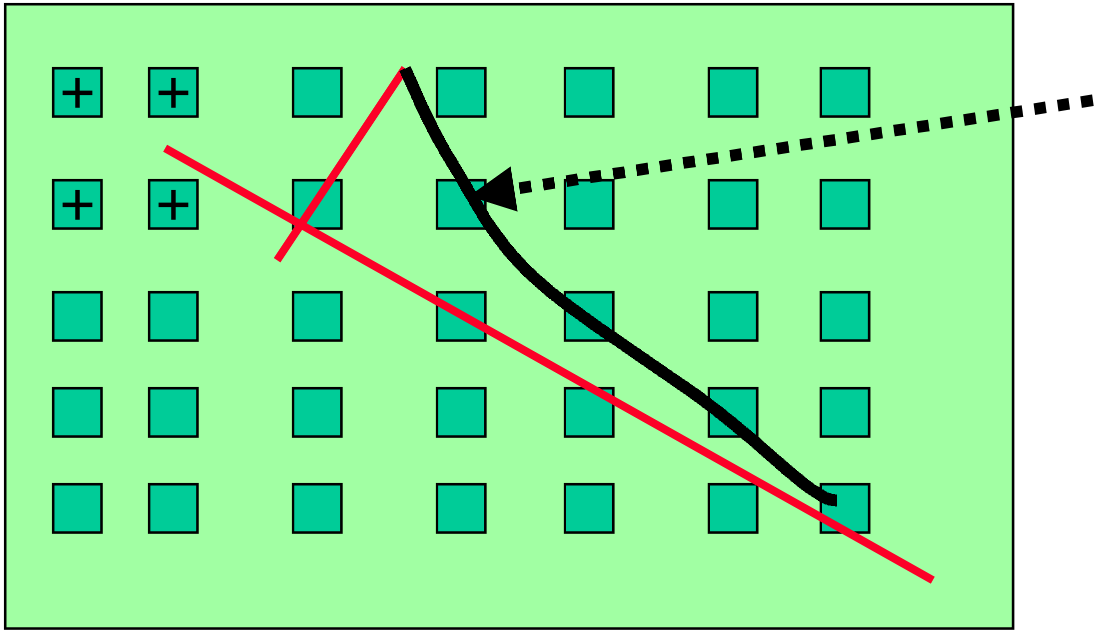
- Everything is electromagnetically coupled to everything else.
- The associated N-port will have N squared interactions.
- The reduced-order model is impossible for circuit simulation.
- Research supported under MARCO Interconnect Center.

Starting with the Substrate Coupling Problem (easiest).



- Noise Coupling problem is a full chip effect.
- Every contact is resistively coupled to every other contact.
- 1 Million contacts, 1 TRILLION resistors

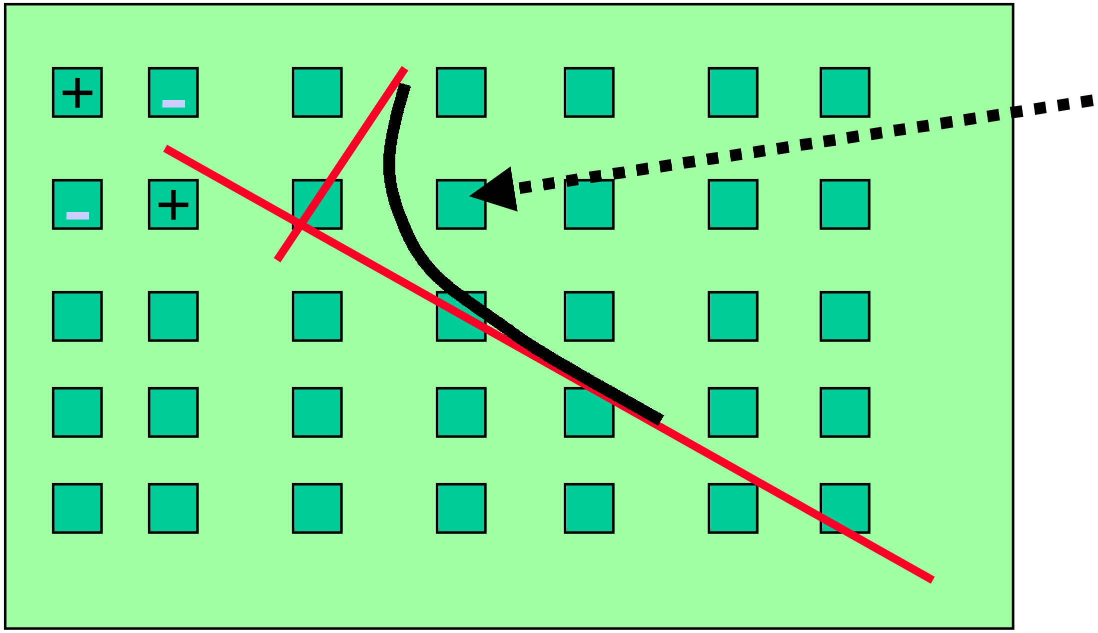
Sparsify Conductance matrix using wavelet change of basis.



Slow Decay in space.

- Coupling between contacts dies slowly in space.
- Coupling between pairs of balanced contacts dies quickly.
- Wavelets generalize the idea, faster fall-off.

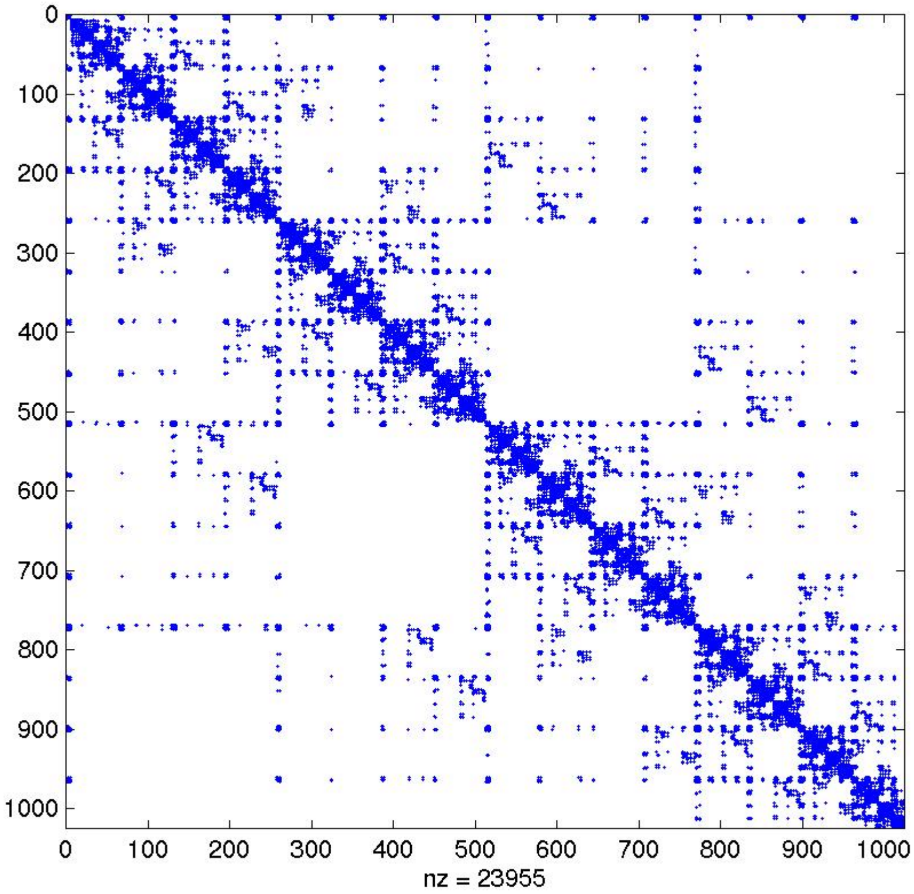
Sparsify Conductance matrix using wavelet change of basis.



Faster Decay
in space.

- .Coupling between pairs of balanced contacts dies quickly.
- Wavelets generalize the idea, faster fall-off.

Some Early Results Using the Wavelet Algorithm



Nonzeros in a 1000 contact problem

Size	Solve Reduction	Matrix Reduction
1024	3	6
4096	8	20

Number of nonzeros in matrix reduced by a factor of 20!

For a copy of this presentation,
please contact Zachary Lemnios at:

MIT Laboratory
Solid State Division
244 Wood Street
Lexington MA 02420-9108

Work#	781 981-7802
Fax #	781 981-5024
Email:	zlemnios@ mit.edu

Breakout Session: Device Technology

Projected Technology Directions

In the next 5-10 year time frame, the electronics device technology will be more CMOS - in all proposed variations - to squeeze out everything possible from the billions of dollars of cumulated investment. However, an integration of silicon technology with MEMS, bio etc., is anticipated (example: neural circuits). Molecular electronics is an emerging technology with carbon nanotubes and organic molecular electronics holding promise; functional circuits and commercially viable technologies are not expected for another fifteen years in this area.

On the optoelectronics side, the drivers for the tera- era information technology are as follows:

Information Transmission: (Terabit-per-second backbone, long- haul networks)

- Access networks at 100s of Gbits per second
- LAN at 10s of Gbits per second
- 1 Gbit ps to the desktop

Information Processing: (Tera-operations per second computers)

- Terabit-ps throughput switches
- Multigigahertz clocks
- Interconnections at 100s Gbits per second

Information Storage: (Terabyte data banks)

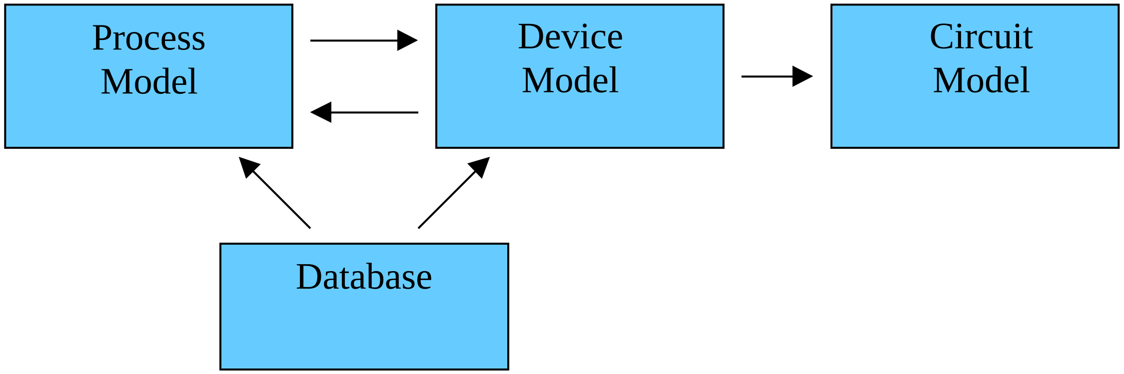
- Mulitterabyte disk drives
- 10s of gigabyte memory chips

Design of Devices/Systems

Regardless of the specifics of the technology discussed in the previous paragraph, "much smaller size" will be the common mantra. Then, the key question is: How does the device work? That is, what is the underlying physics of the device? This question needs to be answered satisfactorily for an effective device and system design. Then, development of quantum mechanical based device simulator will become critical. Whether quantum effect is a barrier (as in aggressive miniaturization of CMOS) or it is clearly exploited to our advantage as in various proposed quantum devices, the need to develop quantum device simulator is clear.

From a utility point of view, the device model or its output should be coupled to a circuit model. A simple tree does not make a forest and a comprehensive quantum model of an isolated device is of no value if the information is not effectively transmitted to and used by a circuit designer. This has been a problem to date and the device and circuit communities don't even seem to have a common language. This barrier has to be overcome and the two groups have to work together.

The next challenge arises from the process complexity and manifests in the strong coupling between processing and device performance. The result is depicted in the schematic below.



Processing results such as dopant distribution and segregation strongly affect device performance. This situation will only be aggravated as device feature size shrinks further and the randomness in doping slowly disappears.

The utility of TCAD is limited without a database that contains information on diffusion coefficients, scattering parameters and all physical and chemical properties. In the era of large devices, it was adequate to evaluate such properties off-line once and make them available during computation in the form of look-up tables, curve fits, model, etc. (e.g. mobility models). But with molecular devices, such information may be dynamically changing during device operation, requiring evaluation of these properties on the go iteratively. As such then, ab initio efforts (density functional theory, tight binding….) need to be coupled to the device and process modeling. This combined approach results in a truly multiscale modeling.

There are several other key issues. The first one is three dimensional modeling which results not only due to miniaturization in all directions but also due to variations arising from 3-d structures such as vertical transistors. In this regard, it is interesting to note that device modeling to date has been primarily done in cartesian coordinates, depicting a nice rectangular box-like device. Future generation CAD must include non orthogonal gridding, adaptive mesh, etc. which have long been utilized in aerospace and automotive TCAD efforts.

Physical issues of critical importance to be considered in the next generation TCAD are as follows. Thermal issues are becoming serious as variations affect properties and device performance and as such, need to be modeled properly. Also, it would become meaningless to model a device in isolation, rather it must be considered along with its surroundings. For example, in ultrasmall devices and in molecular electronics, the contacts dominate and control the device behavior and output. In other words, the definition of a "device" itself becomes broader, that includes a controlling surrounding.

Transient effects in electromagnetics can no longer be ignored. A clear example is a near-THz device (RTD) operating as a high frequency clock. The clock design involves large amplitude excursions between voltage levels below the voltage at peak current, and voltages well into the saturation region. These large signal voltages cannot be adequately handled in the frequency domain but instead require a transient analysis.

Another issue of importance in multilayered quantum structures is the effect of stress. Large mechanical stresses develop within the structures affecting the bandgap. Modeling has to account for the strain within the quantum wells and other lower dimensional structures. These strains may adversely affect the device operation or can be "engineered" to achieve new effects. In any case, future TCAD tools must couple device physics to thermal and mechanical phenomena. Finally, the existing models, though cover silicon, its oxide and nitride, woefully lack information on other materials and hence, coverage of new materials is a must.

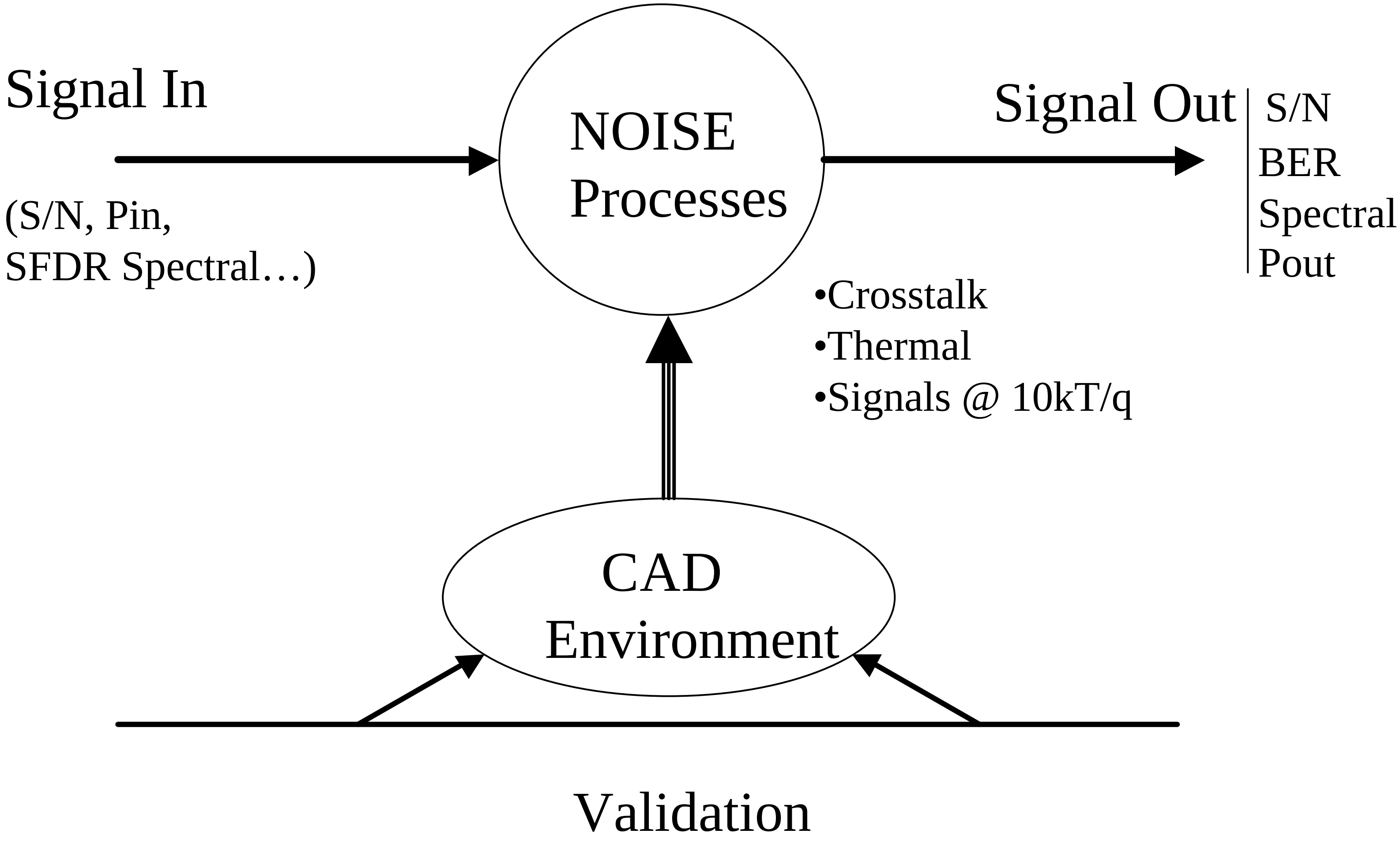
DARPA vs. Industry Investment

In the seventies, eighties, and early nineties, most, if not all investment in device/process modeling, as well as TCAD came from DoD. In the last five years or so, investment in TCAD by the industry is on the rise. This is primarily on CMOS and wouldn't include unique device/system needs by the DoD. For example, the industry doesn't care or worry about 1 fs gitter in an RTD; one can come up with hundred such customized needs by the DoD which cannot be met by COTS technology. Given this, the shrinking contractor base, and the fact there is no existing tools meeting the criteria listed here for the use of DoD and its contractors, an investment from DARPA becomes a necessity.

Integration into Existing Tools

Device modeling tools taking into quantum effects are nonexistent now. It is always possible to add some form of quantum correction into existing classical modeling tools. The impetus to do so arises from the rapid run times of classical models. The disadvantage is that it is only a 'correction' and there is no doubt it will take a significant effort to come up with a right correction and even more effort, to validate it. On the other hand, the available computing power is rapidly increasing and the bold move then would be to go for self-consistent quantum models with necessary ab initio calculations for material properties. However, as pointed out earlier, the output of this must be coupled to circuits. The interfacing may be accomplished through a model reduction.

Breakout Session: Device Integration   CAD Fidelity--Key Metrics



Signal In

(S/N, Pin,
SFDR Spectral…)

NOISE
Processes

Signal Out

- S/N
- BER
- Spectral
- Pout

- Crosstalk
- Thermal
- Signals @ 10kT/q

CAD
Environment

Validation

Environment

- Mechanical
- Electrical
- Optical
- Thermal
- E&M

Tightly coupled,
Easily configurable

Multiple fidelity levels,
Fabrication dependant properties

System-level View

(Choices/Trade-offs w/ Heterogeneous Technology)

Design Tools

{ Efficient
&
Configurable
(see Env. Slide)

Synthesis

(a key goal!)

Technology Driver

10 GHz Application (60 GHz Si-based
"foundry" process)

Silicon Substrate

3D Integration ("x-y-z technologies"):
- *MEMS/Opto-Electronic*
- *Driver for Noise-limited System*

& Environment Constrained…(see Slides [A]& [B])

Breakout session: System-on-a-Chip Technology

- Definition: “System on a Platform SoP”
  - Manufacturable system with diverse physical functions
- Participants:
  - Lawrence Arledge, SRC
  - Bob Brodersen, UC Berkeley
  - Gary Fedder, Carnegie Mellon University
  - Bob Hillman, AFRL
  - Mehdi Kazemi-Nia, Cognet Microsystems
  - Steve Levitan, U. Pittsburgh
  - Mary Ann Maher, MEMSCAP
  - Sharad Malik, Priceton
  - James Murphy, DARPA
  - Marty Peckerar, NRL
  - Joel Phillips, Cadence
  - Jacob White, MIT
  - C.K. Ken Yang, UCLA

- Projected Technology Direction:
  - Combine state-of-the-art CMOS with wild and crazy physics

- Why should DARPA be interested?
  - Sensors & actuators important in almost all future DoD systems
  - Super-high performance (e.g., wideband)

  - Sensors & actuators = Weird physics
    - Commercial world isn’t very interested
    - Supported design flow not available to DoD or to DoD contractors

Challenges and Roadblocks

- **Current CAD does not exploit technology diversity and change!**
  - Mixed-technology: analog, digital, RF, mechanical, fluidics, optical, bio, …
  - No methodology & infrastructure to handle multi-physics systems
  - Lack of standards & support from multi-physics fabs
- **Rapid design (“design in a day”)**
  - First, enter system specification, then
  - Automate, optimize, & implement everything below
- **Complexity; lack of mixed-physics hierarchy**
  - Inadequate or missing modeling methodology & database (IP)
  - Coupled design tradeoffs from device to system
  - Simulation accuracy vs speed tradeoff
- **Architecture-aware tools**
  - Leverage existing trend of state-of-the-art technology (CMOS)
- **Reliability, yield, failure and fault models & simulation**
- **Important Technical Issues:**
  - Noise, multi-domain crosstalk, thermal management, power
- **Lack of commercially available truly leading edge digital design flow**
- **Need DoD-relevant application drivers**

Paradigm shift for designing **mixed-technology** SoC's

- Architecture-aware tools for technology problems
  - Domain-specific system design (with underlying physics and optimization)
  - Generation of application-specific design environments
- System partitioning (3-D planning, choice of technology soln)
- IP based block design
  - Characterization of IP (datasheet)
  - Multi-physics IP (synthesis)
  - Need to build dependable systems from undependable components; need to account for component interactions
- Technology choice (e.g., monolithic vs 3-D chip)
  - Trade-offs: Cost, performance, reliability, power, thermal, noise, …
- Generalized automated modeling paradigms, approaches and tools
  - Physics-based abstract models
  - Coupled problems on a range of scales
  - Nonlinear modeling
  - Built-in error estimation for model and simulation
  - Geometric & manufacturing sensitivities

Metrics

- Availability of leading edge multi-technology design flow for DoD
- Design implementation improvement from 9 months to a day – 270x
  - How?
    - Shove system design through CAD tools
    - Use automation and super-fast algorithms!
- # of Technologies x Domains x Blocks increases from 10 to 1000
- Application-specific improvements in cost, performance, reliability, power, thermal, noise, … of 10-100x
- Nonlinear model generation time reduced from 2 years to 1 week (100x)